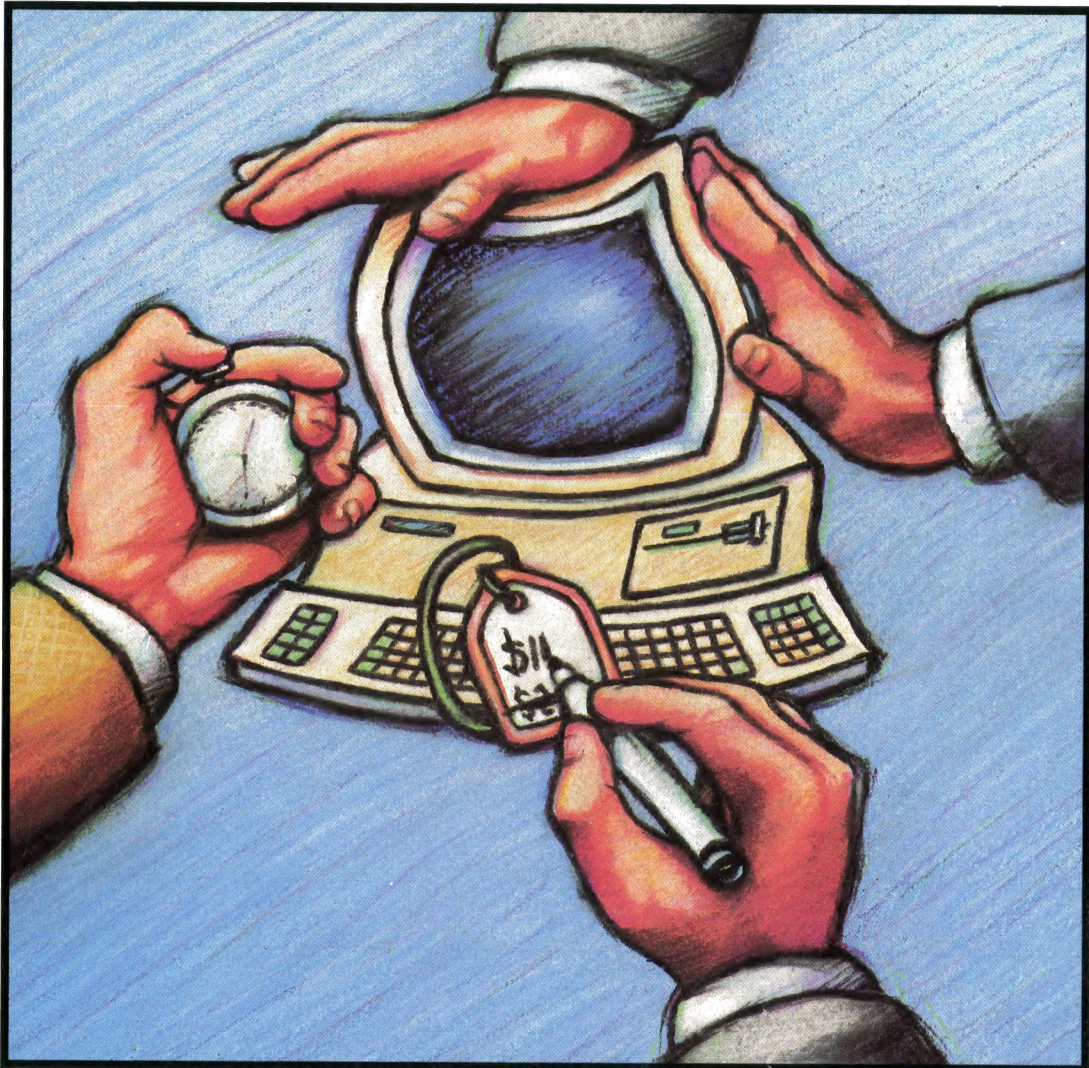


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- Advanced Intel 82385 Cache Memory Controller with 32 KB of high speed static RAM cache.
- Page mode interleaved memory architecture.
- VGA systems include a high performance 16-bit video adapter.
- Socket for 25 MHz Intel 80387 or 25 MHz WEITEK 3167 math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Dual diskette and hard drive controller.
- Enhanced 101-key keyboard.
- 1 parallel and 2 serial ports.
- 200-watt power supply.
- 8 industry standard expansion slots (6 available).

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Prices listed reflect 1 MB of RAM. 322 MB hard drive configurations also available.

*Performance Enhancements (Systems 325, 310, 316 and 220): within the first megabyte of memory, 384 KB of memory is reserved for use by the system to enhance performance.
4 MB configurations available on all systems. Call for pricing.



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Expandable, affordable access to 386 architecture.

STANDARD FEATURES:

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- VGA systems include a high performance 16-bit video adapter.
- LIM 4.0 support for memory over 1 MB.
- Socket for 16 MHz Intel 80387SX math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Integrated high performance hard disk drive interface and diskette controller on system board. (ESDI based systems include a hard disk controller.)
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- 200-watt power supply.
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100 MB VGA Color Plus System	\$3,799
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THE DELL SYSTEM® 220
20 MHz 286.

It's faster than many 386 computers, and has a smaller footprint.

STANDARD FEATURES:

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- Page mode interleaved memory architecture.
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- Socket for Intel 80287 math coprocessor.
- One 3.5" 1.44 MB diskette drive.
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**Lease for as low as \$109/month.
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100 MB VGA Color Plus System	\$3,899

Prices listed reflect 1 MB of RAM. External 5.25" 1.2 MB diskette drive available.

DISCLAIMER: All systems are photographed with optional extras.



THE NEW DELL SYSTEM® 210
12.5 MHz 286.

The price says this is an entry-level system. The performance says it's a lot more.

STANDARD FEATURES:

- Intel 80286 microprocessor running at 12.5 MHz.
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- Page mode interleaved memory architecture.
- LIM 4.0 support for memory over 1 MB.
- Integrated diskette and high performance 16-bit VGA video controller on system board.
- Socket for Intel 80287 math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Integrated high performance hard disk interface on system board.
- Enhanced 101-key keyboard.
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20 MB VGA Monochrome System	\$1,699
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40 MB VGA Color Plus System	\$2,199

Prices listed reflect 512 KB of RAM.

†† 640 KB versions of the above systems are available for an additional \$80.
100 MB hard drive configurations also available.

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- Page mode interleaved memory architecture.
- VGA systems include a high performance 16-bit video adapter.
- Socket for 20 MHz Intel 80387 or 20 MHz WEITEK 3167 math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Dual diskette and hard drive controller.
- Enhanced 101-key keyboard.
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- 200-watt power supply.
- 8 industry standard expansion slots (6 available).

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Prices listed reflect 1 MB of RAM. 150 and 322 MB hard drive configurations also available.

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And just as we can custom configure your computers, we can see to it you get a custom designed lease plan to fit the exact needs of your business.†

It's just another example of why over half the Fortune 500 companies now own or lease Dell systems.

And why you may decide that from now on, the only place you'll go to buy a computer is the phone on your desk.

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to find a better
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package for the
power user that is
lurking inside you."*

November 29, 1988



OUR SYSTEM 310 IS FASTER THAN A BAT OUT OF HELL.



If you've been looking at 386™-based computers, you obviously feel the need for speed.

Something the Dell System® 310 delivers in spades.

In fact, the System 310 has more speed than even the most seasoned 386-users have come to expect. Case in point, PC Labs benchmark tests. The System 310 consistently outperformed

the Compaq^ 386/20e. Not to mention the IBM PS/2^ Model 70-121. Leading one reviewer to comment, "It's fast enough to burn the sand off a desert floor."

For us, however, fast enough is not enough. By utilizing an Intel® 82385 Cache Memory Controller, page mode RAM and interleaved memory, the 310 not only delivers the aforemen-

tioned speed, but enough horsepower to do everything from CAD/CAM to megaspreadsheets to databases the size of the Manhattan Yellow Pages.

It even has the umph to work as a network file server.

TELL US WHAT TO DO NEXT.

As much as the System 310 has to offer, it doesn't even begin to reach its full potential until after we've heard your input.

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Storage? You can have a 40 MB hard disk drive. Or choose a 100, 150, or 322 MB hard drive.

The System 310 comes standard with 1 MB of RAM. Want more? We can configure up to 8 MB on the system board.

Still not enough? We can add another 8 MB by installing a high-speed memory expansion board. You can even run your System 310 as either a MS-DOS®, MS®-OS/2 or UNIX® system.

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The point here is that when you order a System 310, you not only get a 386-based system that's incredibly fast, powerful and versatile, but incredibly personal as well.

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To a sophisticated computer user, there's nothing worse than having to buy from a retailer who knows little more than you do.

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Because, after all, computer retailers are in the retail business first. And in the computer business second. So expecting expert advice on computers is asking a lot.

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One of the things that very clearly sets Dell systems apart from other computers is not just how they're sold but how they're supported.

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As you've probably guessed by now, one of the things that drives us most is customer satisfaction.

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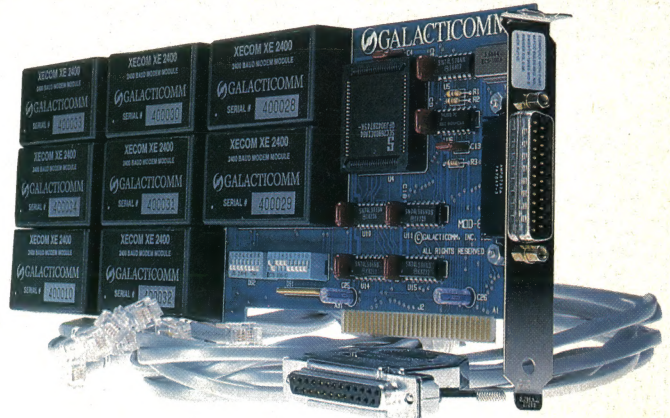
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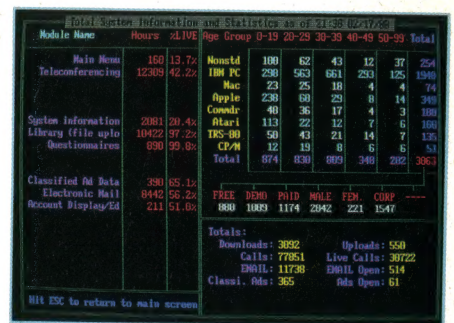
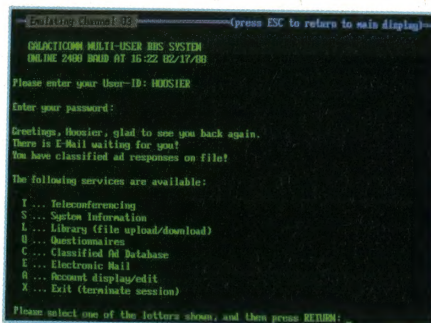
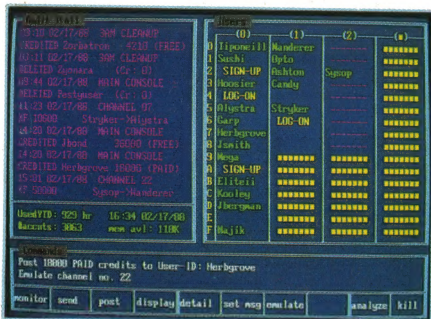
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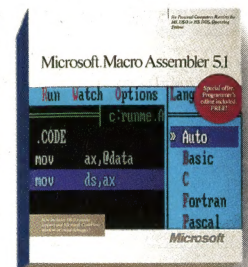
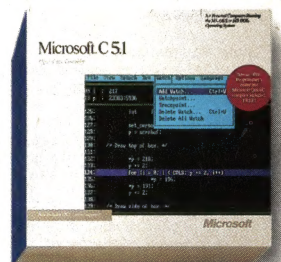
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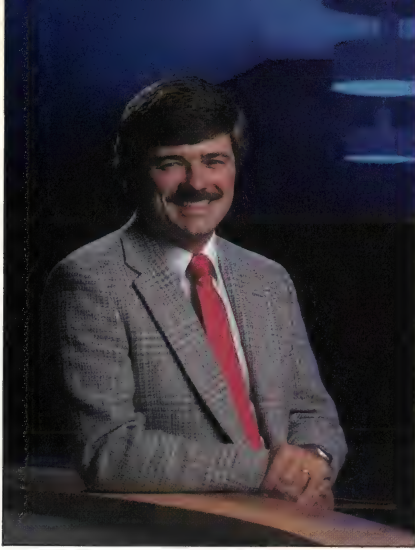
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MORE BANG FOR YOUR BUCKS

New 80486-based systems from Cheetah and ALR prove that high-performance hardware doesn't have to cost a fortune

Several months ago, I crossed my fingers for luck and wrote, "We may see the 80486 market split in two radically different directions: killer systems with killer prices for departmental computing needs, and relatively inexpensive fast systems for personal desktop use."

In this industry, one of the safest things that you can do is to predict high prices. But fortunately for me (I don't like the taste of crow), Cheetah and ALR delivered on the low-price prediction. Their machines could trigger a major reshuffling of prices across all Intel-architecture machines.

Cheetah's new 25-MHz 80486 tower system is based on the motherboard it showed last spring (see the June and August editorials). The entry-level version of the new system comes with 4 megabytes of RAM, a 60-megabyte hard disk drive, a VGA controller, a monochrome VGA monitor, and a 1.2-megabyte 5¼-inch floppy disk drive. For this, you pay just \$4995.

ALR's PowerFlex is based on its attractive \$1495 12-MHz 80286 system that comes standard with a 40-megabyte hard disk drive and 1 megabyte of RAM. With the addition of a \$2995 plug-in module, it becomes a \$4500 80486-based system, albeit one with a 16-bit data bus; sort of an 80486SX.

Stunning Price and Performance

In absolute terms, \$4500 or \$5000 is still a fair chunk of change. But in terms of

relative pricing, or better still, price/performance, these systems represent a stunning advance.

Maybe "stunning" sounds like hyperbole. After all, there are no "real" 80486 machines yet: Every system we've seen so far is built around a prototype motherboard carrying a prototype ("A" Step) CPU chip.

But from the early benchmarks, we're confident that the production-model Cheetah 80486 systems will outpace many, and maybe all, of the current crop of 33-MHz 80386-based systems. For example, the Everex Step 386/33—a very nice machine—turns in CPU, FPU, and video benchmark indexes of 6.84, 15.48, and 4.26, respectively (where an 8-MHz AT equals 1). The preproduction 25-MHz Cheetah already yields 6.52, 21.49, and 5.57, respectively.

At its introductory price, the Cheetah's cost is only about half that of the next-least-expensive 80486-based box. I'd call that "stunning."

The ALR system, with its AT-bus bottleneck, isn't nearly as fast as the Cheetah, or any 80486 with a full-width data path: Its preliminary CPU, FPU, and video benchmark indexes are 4.18, 21.85, and 3.80, respectively.

But the ALR system also isn't nearly as costly as most other 80486-based systems: The ALR system is simply the world's least-expensive 80486, period. For some non-I/O-intensive software, we expect that the PowerFlex 486 will easily keep up with machines costing two and even three times as much. "Stunning?" You bet.

EISA on the Way

BYTE's November issue will have a complete First Impression and preliminary benchmarks of the Cheetah and ALR 80486 systems.

We're also planning coverage of three other 80486-based machines, including what will be the first announced EISA-bus machine. (Yes, a brand-new bus and

a brand-new chip in the same machine.) The story is currently under a strict embargo, so we can't release the name of the manufacturer yet; but I'll bet that you will be surprised when you see just who it is.

In any case, the appearance of a relative "low end" in 80486 machines is a welcome development. Cheetah and ALR have done us all a favor.

For one thing, the aggressive prices announced by Cheetah and ALR place immediate pressure on the high-priced 80486 vendors. To justify the extra costs, 80486 vendors will have to be sure they've added meaningful extra value beyond the pizzazz of simply having an 80486 chip inside.

Aggressive low pricing may even advance the date when 80486 price wars break out.

Big Ripples

And the ripple effects will be profound. Consider that an 80486 chip, with its on-board FPU and cache, outperforms and currently costs less than a 33-MHz 80386 with separate FPU and cache chips. Very simply, for the 80386 chip to survive, 80386 machines will have to drop to a price point well below that of similarly equipped 80486 systems. With Cheetah and ALR already drawing the lower boundaries of 80486 pricing, vendors of fast 80386 systems now have a clear target to beat.

There will always be a place for departmental "killer" systems that only a corporate budget can afford. But these first low-cost 80486 machines may help lower all 80x86 system prices back down toward the range where personal computing can become personally affordable again.

Systems like these two from Cheetah and ALR may be just what the doctor ordered.

—Fred Langa
Editor in Chief
(BIX name "flanga")



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Not too long ago, a few dozen people sharing the same programs, resources, and information on a single computer at the same time meant only one thing—a mainframe.

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Then along came the latest generation of personal computers. And now, the same people are more and more likely to be found doing exactly the same things—simultaneously sharing programs, resources, and information—on a PC.

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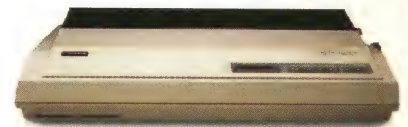
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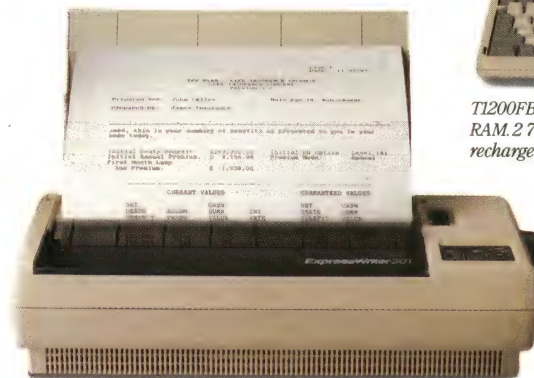
T1000: 6.4 lbs, 4.77MHz 80C88, 512KB RAM expandable to 1.2MB. MS-DOS in ROM, 720KB 3 1/2" diskette drive. Built-in RGB, parallel, serial and external drive ports.



P341SL: Wide carriage (up to 270CPL), 216/72 cps, advanced paper handling, 4 part forms.



T1200FB: 9.8 pounds, 9.54MHz 80C86, 1MB RAM. 2 720KB 3 1/2" floppy drives, removable/rechargeable battery pack.



ExpressWriter 301: 4 lbs, letter-quality 24-dot print head, 60 cps, Toshiba/Qume and Epson LQ emulations, 5 resident fonts.



T3100e: 12MHz 80286, internal IBM slot, 20MB hard disk, gas plasma display, 1MB RAM expands to 5MB, 1.44MB 3 1/2" diskette drive.



T5100: 16MHz 80386 microprocessor, 40 or 100MB hard disk, 2MB RAM expandable to 4MB. 14.6 lbs. Built-in EGA display with high resolution gas plasma screen.



P351SX: 360/120 cps, 24-pin letter quality, color option, Toshiba/Qume and IBM emulations standard, Epson & Diablo emulations optional.

great minds don't think alike.



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T5200: 20MHz 80386 processor, 2 internal IBM compatible expansion slots, 40 or 100MB hard disk, VGA display with external VGA monitor port, 2MB RAM expandable to 8MB.



T3200: 12MHz 286, 2 IBM compatible slots, 40MB hard disk, 1.44MB floppy, 1MB RAM expands to 4MB, EGA screen.



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ExpressWriter 311: 24-pin dot matrix, 180 cps draft/60 cps letter quality, 3 resident emulations (Toshiba/Qume, Epson LQ, IBM Proprinter), 16K buffer, 5 resident fonts plus card slots, 11 lbs.

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TI200HB: 10.8 lbs, 9.54MHz 80C86, 20MB hard disk, 1MB RAM, includes 384KB LIM-EMS. Removable/rechargeable battery pack.



P321SL/SLC (color): 216/72 cps, 24-pin letter quality, up to 360x360 DPI graphics. Toshiba/Qume and IBM emulations standard, Epson and Diablo emulations optional, 32KB print buffer, front panel controls, advanced paper handling.

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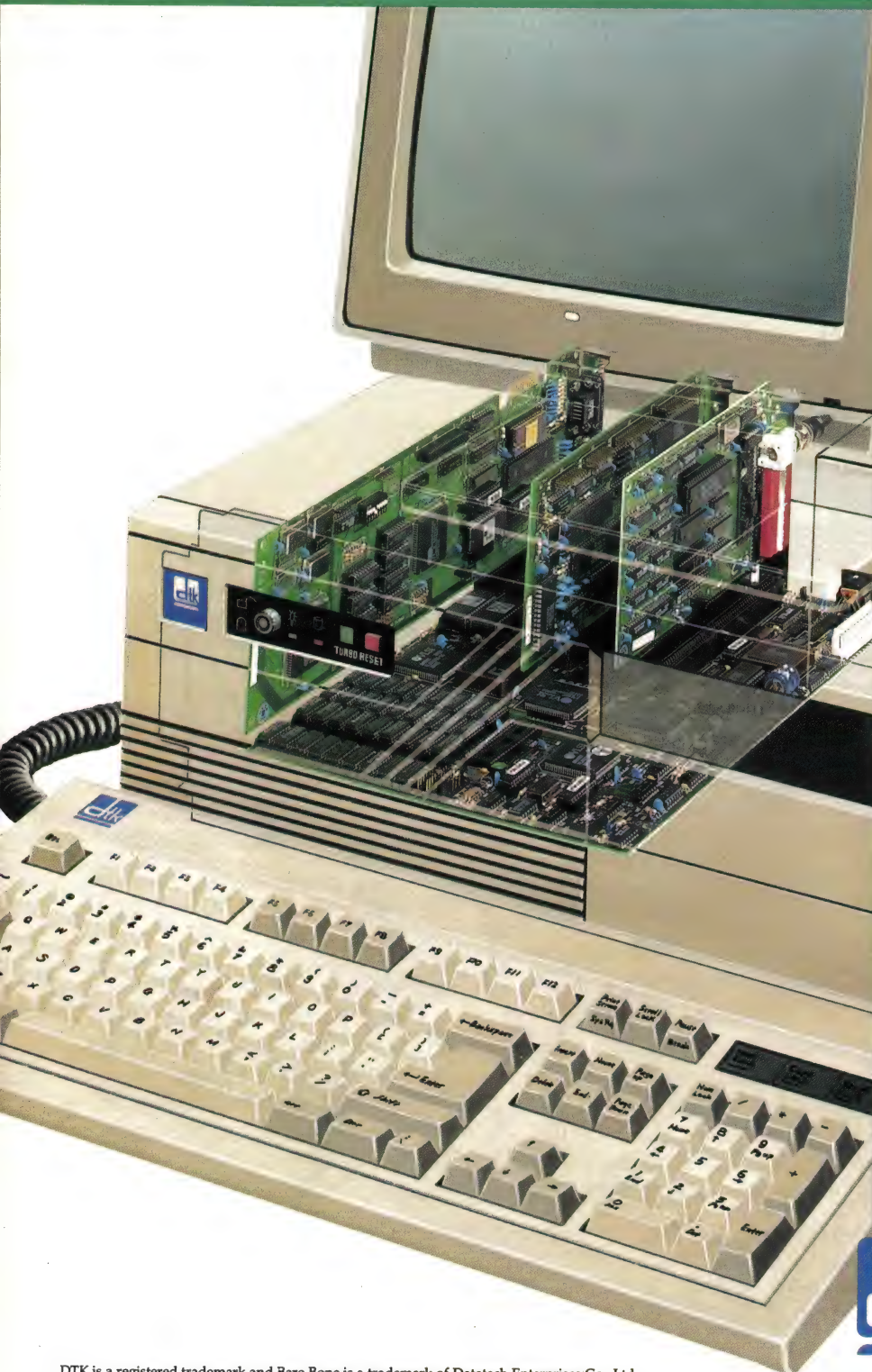
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Circle 89 on Reader Service Card (DEALERS: 90)

MEGAHERTZ MADNESS

BYTE editors

check out **15** of the world's
fastest PCs

For the last couple of months, BYTE has received a steady stream of press releases touting the virtues of the latest "world's fastest PC." Since Intel began shipping its 33-MHz version of the 80386 CPU, PC makers have hustled to get it into their systems in the hope that a magazine like BYTE will award them that title. We would like to oblige, but the task is more complicated than it first appears.

BYTE received 14 33-MHz PCs and the new Unix-based Altos 80386 system (see the text box "Altos 386 Series 1000: For Unix Only" on page 30). We benchmarked them all. We can tell you which one had the fastest CPU (the Everex Step 386/33) and which one had the best overall application index (the SIA 386/33). But when you run applications that are not CPU-intensive or change the system configuration, those rankings become less meaningful.

A fast CPU will always be a fast CPU, but it won't make your hard disk drive access data any faster. For a better application index score, all you have to do is install a good disk-caching controller with lots of memory—expensive, but the results are impressive.

The "world's fastest PC" is the one that lets you finish your work in the least amount of time. Since this is what the BYTE application index measures, the SIA 386/33 has the most right to the claim. But then, no other PC in this group had a 4.5-megabyte hard disk cache, which dramatically improves performance for disk-intensive applications. When reading the descriptions of each machine, remember that every PC here, even the SIA 386/33, could have received better application index scores by using faster I/O interfaces, increasing the size and speed of the CPU and disk caches, or using faster hard disk drives. It's just a matter of how much money you want to spend.

Speaking of Money

We have compiled several tables so you can more easily compare the systems. Tables 1 and 2 list the features of each system's base model. The configuration and model designations

for the units we received may vary from the entries in the tables. Some systems start at a very low price but offer little more than a keyboard, a case, a motherboard and memory, and a floppy disk drive. Two, the Dyna Cache 386 and the Tangent 333, don't have standard models at all; the companies custom-configure each unit to the buyer's specifications.

Higher-priced units offer more in the way of hardware, and they often carry a well-known brand name. You pay a premium for a computer from a company with an established reputation that can presumably provide greater system reliability and better customer support. But buying from a lesser-known company can save you several thousand dollars—an important factor for those with a limited budget.

Keep in mind, too, that the prices we give in this roundup are the manufacturers' retail prices. Retailers, value-added resellers (VARs), and mail-order houses may have lower prices.

We've omitted some obvious categories from tables 1 and 2 because all vendors offer the same type of feature. For instance, all systems come with a 1.2-megabyte 5¼-inch floppy disk drive standard (a few will swap it for a 1.44-megabyte 3½-inch floppy disk drive if you wish), and all systems accept either an Intel 80387 or a Weitek 3167 math coprocessor. Each system allows you to change the CPU speed setting, and all the systems will run OS/2 or a variety of Unix given sufficient RAM and hard disk capacity.

Table 3 and figure 1 give the BYTE benchmark indexes. When looking at the rankings, it's important to maintain perspective. Even the slowest 33-MHz PC is over 20 times faster than an IBM PC AT on the application index. In fact, it's about 20 percent faster than the fastest machine that IBM currently offers. Speed is wonderful, but other factors, such as expandability, construction quality, and price, are just as important.

Wonderful, Yes; But Who Needs It?

Buying a barn-burning 33-MHz PC for everyday office grunt work is silly; relatively simple tasks such as word processing

continued

Table 1: Main system features, price, and warranty. Price variations are due mainly to differences in what's offered in the standard configuration. Note that most vendors use third-party motherboards; variations in performance among systems using the same motherboard are possible by using faster I/O controllers and devices, larger and faster caches, and faster memory.

Computer	Price	Motherboard maker	RAM				ROM BIOS	Power supply	Warranty
			Standard memory	Access time	Max. RAM	RAM cache			
ALR FlexCache 33/386 Model 150	\$9990	ALR	2 Mb	60 ns	16 Mb	128K; 25 ns	Phoenix	200 W	1 year
AST Premium 386/33 Model 115V	\$8495	AST	2 Mb	80 ns	36 Mb	32K; 25 ns	AST	220 W	1 year
Blackship 386/33	\$4195	Micronics	1 Mb	80 ns	16 Mb	32K; 25 ns	Phoenix	220 W	1 year
Compaq Deskpro 386/33 Model 84	\$10,499	Compaq	2 Mb	80 ns	16 Mb	64K; 25 ns	Compaq	300 W	1 year
Dyna Cache 386 ¹	\$9993	AMI	4 Mb	70 ns	16 Mb	64K; 20 ns	AMI	275 W	1 year
Everex Step 386/33	\$7599	Everex	4 Mb	100 ns	16 Mb	64K; 20 ns	Phoenix	200 W	1 year
FiveStar 386 Model 333	\$3395	Micronics	1 Mb	80 ns	16 Mb	32K; 25 ns	Award	200 W	1 year
Matrix MDP 386-33	\$5585	Micronics	4 Mb	80 ns	16 Mb	32K; 25 ns	Phoenix	275 W	1 year
Micro Express ME 386-33	\$5995	AMI	4 Mb	70 ns	16 Mb	64K; 20 ns	AMI	220 W	15 months
National MicroSystems Flash 386-33	\$4999	Micronics	4 Mb	80 ns	16 Mb	64K; 25 ns	Phoenix	200 W	1 year
PC Link 386/33 Model 160	\$5995	Hauppauge	4 Mb	80 ns	64 Mb	64K; 20 ns	Award	220 W	1 year
SIA 386/33	\$6490	AMI/SIA ²	4 Mb	70 ns	16 Mb	64K; 20 ns	AMI	350 W	1 year
Tangent 333 ¹	\$6995	Mylex	4 Mb	80 ns	32 Mb	128K; 25 ns	AMI	250 W	1 year
Zenith Z-386/33 Model 150	\$11,499	Zenith	2 Mb	80/100 ns	64 Mb	16K; 15 ns	Zenith	200 W	1 year

¹ No standard model; systems are built to customer's specifications. Configuration shown represents system sent to BYTE.

² AMI customizes its 33-MHz motherboard for faster memory to SIA's specifications.

Table 2: Standard storage, video, I/O, and expansion features, plus bundled software and FCC ratings. Hard disk storage and controller type vary considerably, although in virtually all cases it is possible either to specify the drive and controller type of your choice or to buy a stripped system and install your own. When considering expansion slots, keep in mind that on most systems at least one slot is occupied by a video, memory, CPU, or controller card. Systems that integrate these functions onto the motherboard may have fewer slots, but the same or greater expansion capability. Most vendors sell the operating system at extra cost, often offering a choice of MS-DOS or OS/2. An FCC rating of A means that the machine is certified for use only in business environments; B is certification for home or residential use.

Computer	Hard disk drive						Case type ¹
	Controller type	Hard disk maker	Access time	Capacity	Hardware cache?	Max. # bays	
ALR FlexCache 33/386 Model 150	ESDI	Maxtor or CDC	17 ms	150 Mb	No	5	T
AST Premium 386/33 Model 115V	AT	Imprimis	16 ms	110 Mb	Yes	5	D
Blackship 386/33	AT	Seagate	28 ms	40 Mb	No	5	D
Compaq Deskpro 386/33 Model 84	AT	Conner	25 ms	84 Mb	No	5	D
Dyna Cache 386 ⁴	ESDI	Micropolis	18 ms	147 Mb	No	6	T
Everex Step 386/33	AT	Option	—	—	No	5	D
FiveStar 386 Model 333	Option	Option	—	—	Option	5	D
Matrix MDP 386-33	AT	Option	—	—	No	5 ⁵	T
Micro Express ME 386-33	ESDI	Option	—	—	Yes	5	D
National MicroSystems Flash 386-33	ESDI	Option	—	—	Yes	5	D
PC Link 386/33 Model 160	ESDI	Micropolis	17 ms	159 Mb	No	5	D
SIA 386/33	Option	Option	—	—	Option	10	T
Tangent 333 ⁴	ESDI	CDC	18 ms	100 Mb	No	10	T
Zenith Z-386/33 Model 150	ESDI	MiniScribe	18 ms	150 Mb	No	4	D

¹ D=desktop; T=tower.

² a=MS-DOS 3.3; b=MS-DOS 4.xx; c=system setup software; d=disk-caching utility; e=system utilities; f=Microsoft Windows.

³ Game port.

⁴ No standard model; systems are built to customer's specifications. Configuration shown represents system sent to BYTE.

⁵ Two bays accept only 3 1/2-inch devices.

perform only slightly faster at 33 MHz than they do at 12 MHz. Place a 33-MHz machine in front of an engineer, financial analyst, or software developer, though, and you've made a friend. Fill a 33-MHz PC with a few hundred megabytes of hard disk storage and the right networking hardware, and you have a powerful file server for a LAN or multiuser environment. Combine a 33-MHz machine with a laser printer and imaging hardware, and you get a fast workstation suitable for desktop publishing.

With a 33-MHz PC, you can expect to shave 20 percent to 30 percent off the CPU processing time of a 25-MHz PC. The longer your application takes to process, the greater the benefit. Switching to a faster processor might save you seconds, minutes, or even hours. For some tasks, even the most expensive 33-MHz PC could pay for itself in the time it saves.

ALR FlexCache 33/386

Advanced Logic Research's 33-MHz entry sports a unique tower design. Remove the side panel and you see a large swing-arm on which the hard disk drive is mounted. The advantage is twofold: The arm's full-height hinge and an accompanying brace on the other side add much-needed rigidity to the ALR's otherwise flimsy case, and swinging out the hard disk drive provides easy access to the rest of the FlexCache 33/386's internals.

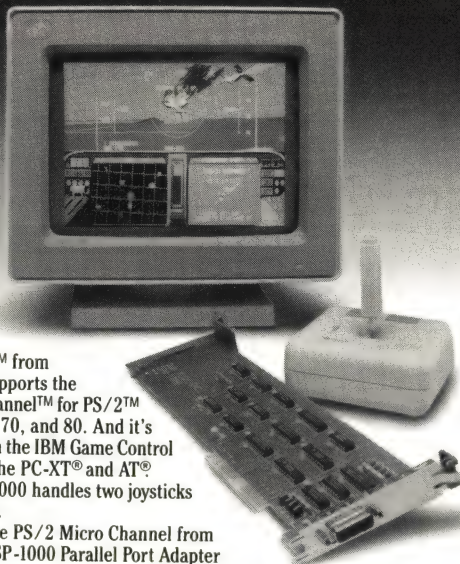
The brace, however, is a pain to reinstall. Although held in

continued



Video		Expansion slots			Ports			Software included ²	FCC rating
Graphics board	Monitor	8-bit	16-bit	32-bit	Parallel	Serial	Mouse		
16-bit VGA	Option	1	7	0	2	1	0	a,c,d	A
16-bit VGA	Option	1	3	3	1	2	0	a,c,d,e	B
Monochrome	Monochrome	2	5	1	2	2	0 ³	c,e	B
VGA	Option	1	6	1	1	2	1	d,e	B
16-bit VGA	VGA	1	6	1	2	1	0 ³	e	A
Option	Option	2	6	0	1	1	0	a,c,d,e	B
Option	Option	2	5	1	1	2	0	—	A
Option	Option	2	5	1	1	2	0 ³	g	A
Option	Option	1	6	1	1	2	0	a,e	B
Option	Option	2	5	1	1	2	0	e	B
16-bit VGA	Option	1	6	1	1	1	0	a or b,c,e	A
Option	Option	1	6	1	1	1	0	c,e	A
16-bit VGA	VGA	1	4	2	1	2	0 ³	a	A
VGA	Option	0	3	4	1	2	0	a,e,d,f	B

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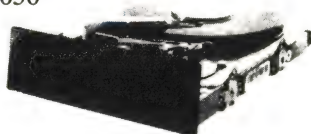
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Table 3: (a) The BYTE low-level benchmark indexes, sorted from highest to lowest CPU rating. Of these numbers, the disk I/O index had the greatest influence on the cumulative application indexes.

Computer	CPU	FPU	Disk I/O	Video
Everex Step 386/33	6.84	15.48	2.45	4.26
ALR FlexCache 33/386	6.74	15.66	2.60	2.83
SIA 386/33	6.27	14.97	8.99	3.27
Compaq Deskpro 386/33	6.09	15.50	2.90	4.53
National MicroSystems Flash 386-33	6.06	15.07	6.48	2.01
Blackship 386/33	6.03	13.71	2.37	3.61
Matrix MDP 386-33	5.75	15.07	1.93	5.73
FiveStar 386 Model 333	5.74	15.75	7.14	2.22
Tangent 333	5.73	14.83	2.28	1.79
Dyna Cache 386	5.67	14.86	2.56	3.85
Micro Express ME 386-33	5.66	15.06	7.02	2.97
PC Link 386/33 Model 160	5.10	14.87	2.83	2.11
AST Premium 386/33	4.80	14.21	2.32	3.89
Zenith Z-386/33	4.79	15.10	2.96	5.05

place by only two screws, the housings for the mass storage devices fit into notches on the brace's backside. The edges of those housings are fitted with plastic strips that immediately fall off when you remove the brace. Replacing them can get tedious if you frequently tinker inside the machine.

But this is a minor annoyance, especially in light of the FlexCache 33/386's superb performance in the BYTE benchmark tests. With a 6.74 CPU index, it is the second-fastest PC we've ever tested, CPU-wise, after the Everex Step 386/33. Its cumulative application index of 24.02 is a respectable one, especially considering that it doesn't have a hardware disk cache. ALR has historically taken performance seriously, and the FlexCache 33/386 certainly reflects that attitude.

ALR designed most of the electronics inside the FlexCache 33/386, the only exceptions being the ESDI disk controller (Adaptec or Western Digital), the 200-watt power supply, and the drives themselves. The motherboard was free of engineering wire changes.

The ALR FlexCache, in its base configuration, comes with a 150-megabyte 17-millisecond Maxtor or Control Data hard disk drive, a 1.2-megabyte 5¼-inch floppy disk drive, an ALR 16-bit VGA card, 2 megabytes of 60-nanosecond RAM (expandable to 16 megabytes), 128K bytes of 25-ns cache RAM, room for another four half-height storage devices, and MS-DOS 3.3. The base unit price is \$9990.

The unit has eight expansion slots: one 8-bit and seven 16-bit. Three slots are taken by the hard disk drive controller, a serial/parallel port card, and the VGA card. Memory goes on the motherboard in single in-line memory module (SIMM) slots for up to 16 megabytes.

The unit BYTE received had a 380-megabyte Maxtor drive, an Adaptec ESDI controller, 4 megabytes of RAM, an ALR VGA II monitor, and a 33-MHz 80387 math coprocessor. This configuration costs \$14,587.

If you need a fast computer, the ALR FlexCache 33/386 is worth your consideration.

—Michael E. Nadeau
continued

(b) The BYTE cumulative application indexes, sorted from highest to lowest. These numbers give an idea of what kind of performance for a given application you can expect in comparison to an IBM PC AT. The rankings are quite different from the low-level results, which measure performance at the system level.

Computer	Word processing	Spreadsheet	Database	Scientific/engineering	Compilers	Cumulative*
SIA 386/33	5.49	4.32	8.09	7.42	7.32	32.64
Micro Express ME 386-33	4.76	4.32	5.83	7.12	5.55	27.58
National MicroSystems Flash 386-33	5.08	4.35	5.77	6.00	5.37	26.58
FiveStar 386 Model 333	4.82	4.31	5.91	5.90	5.53	26.47
Compaq Deskpro 386/33	4.28	5.01	3.00	7.86	4.46	24.61
Dyna Cache 386	5.02	4.27	2.91	7.51	4.42	24.13
ALR FlexCache 33/386	4.61	4.50	2.88	7.18	4.86	24.02
Blackship 386/33	4.69	4.45	2.89	7.30	4.44	23.77
AST Premium 386/33	4.11	4.22	3.01	7.23	4.11	22.69
Everex Step 386/33	4.43	3.93	1.96	8.05	4.25	22.62
PC Link 386/33 Model 160	5.03	4.43	2.68	5.51	4.36	22.01
Tangent 333	4.57	4.45	2.45	5.43	4.27	21.17
Zenith Z-386/33	3.91	3.97	1.87	6.59	3.85	20.19
Matrix MDP 386-33	3.95	3.90	1.74	7.09	3.43	20.11

* Cumulative application index based on indexes at left.

BYTE BENCHMARK RESULTS

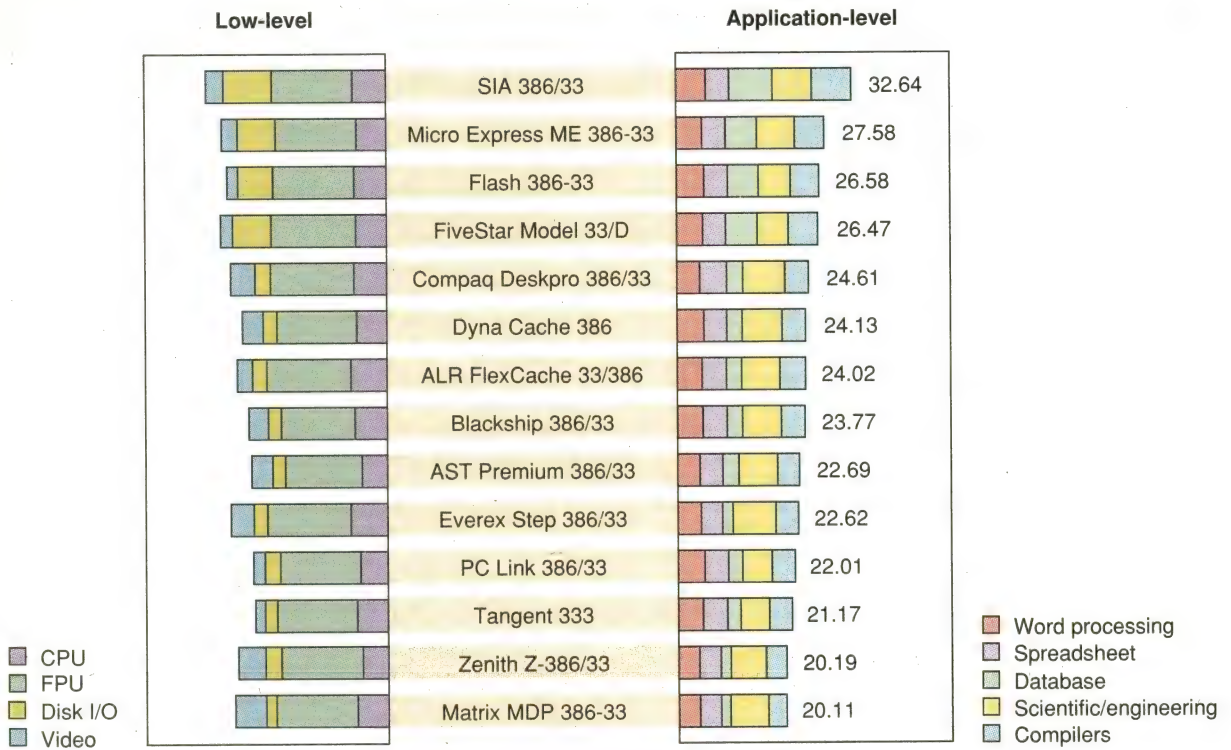


Figure 1: The systems that used the Distributed Processing Technology disk-caching controller took the top four spots on our cumulative application indexes, followed by the Compaq Deskpro. Installing a hardware disk cache in any of the other 33-MHz PCs would dramatically increase their scores, although expensively and sacrificing some hard disk capacity.

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MEGAHERTZ MADNESS

AST Premium 386/33

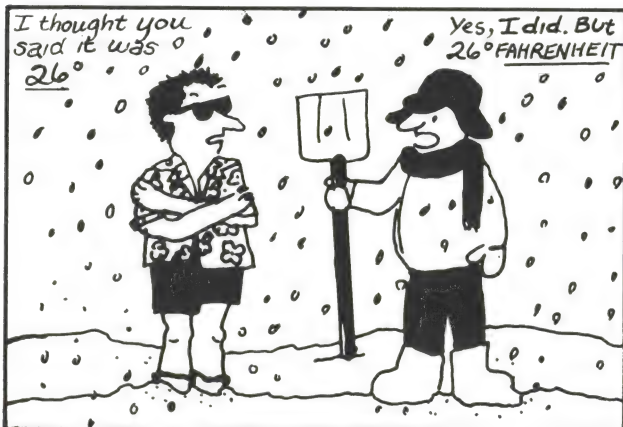
With "Premium" as its middle name, AST's 33-MHz entry has an image to live up to. The AST Premium 386/33 does this nicely with its clean, integrated design, solid construction, and proven components. An \$8495 base price further enhances its high-quality image.

Its performance, however, is about average compared to the other machines tested here. AST includes a disk-caching utility that dramatically improves disk performance, though at the cost of extended RAM. I allocated the maximum 1 megabyte of RAM to the disk cache, which improved the BYTE disk I/O index score nearly sixfold. A 16K-byte RAM track buffer is standard.

The AST-designed motherboard integrates items usually found on separate cards: a parallel port and two serial ports, and the AT-style floppy and hard disk drive controllers. The system's 32K-byte RAM cache is also integrated into four logic chips, including memory. The AST 386/33 has seven slots instead of the usual eight. Two of those slots are taken by the optional AST VGA card and the CPU card. The five remaining slots should meet most users' needs, considering the devices that are integrated on the motherboard. The unit comes with setup software that allows you to disable these devices should you want to install your own.

Only Zenith offers more 32-bit expansion slots than AST (four versus three). Both machines allow for placing AT-type cards or proprietary 32-bit memory cards in those slots.

The CPU card contains the CPU, FPU, up to 4 megabytes of 80-ns SIMM RAM, and the 80325 cache controller. Additional memory, up to a total of 36 megabytes, requires proprietary memory cards from AST. Conceivably, this design could permit easy upgrading should, heaven help us, a faster CPU become available. The rugged metal case is about 1 1/2 inches narrower than those of most other desktop 33-MHz PCs we tested, thanks to the space-efficient integrated motherboard.

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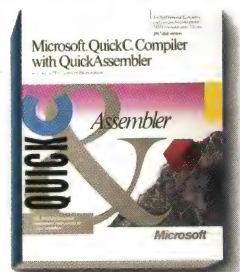
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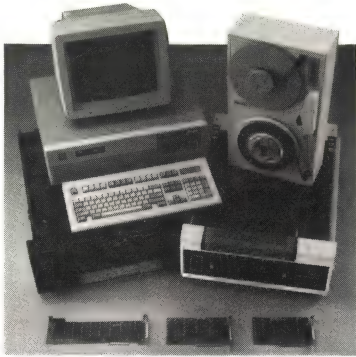
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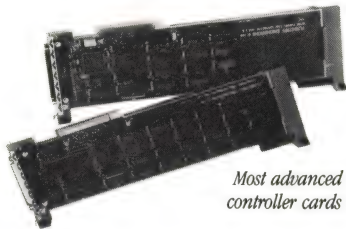
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Our test unit came with a 110-megabyte Rigidyne (Control Data) 3½-inch hard disk drive, a TEAC 1.2-megabyte floppy disk drive, an AST VGA card and Premium Display/VGA monitor, a 33-MHz Intel 80387 FPU, MS-DOS 3.3, and a total of 4 megabytes of 80-ns SIMM memory. The total estimated cost for this system (AST does not offer a math coprocessor; 33-MHz 80387s sell for about \$1000) is \$11,828.

I had no problems using the machine with a Microsoft Mouse and card, and an NEC CDR-77 CD-ROM reader and its SCSI controller. The Premium 386/33 ran Windows 2.0, Lotus 1-2-3 release 3.0, XyWrite 3.51, a finicky public domain fractal program, and NEC's Clip-Art 3D, a Windows-based graphics library on CD-ROM. Compatibility seems good with the AST.

The Premium 386/33's main selling points are its high-quality design and AST's track record as a vendor of solid, reliable hardware. Unless you must have either the fastest or the cheapest 33-MHz PC, the Premium 386/33 should be among your top choices.

—Michael E. Nadeau

Blackship 386/33



Here's a reasonably priced system that performed well. Like several other systems that we tested, the Blackship 386/33 uses the Micronics motherboard. It includes a RAM cache that really speeds things up. I tried several informal tests using two CPU-intensive programs, AutoCAD and MapInfo. With the cache on, which is the default mode for the system, the Blackship performed 27 percent to 42 percent better than with the cache off. (All benchmark tests were run with the cache on.)

The basic system comes with a 33-MHz 80386, a Phoenix BIOS, 1 megabyte of 32-bit RAM, a 1.2-megabyte floppy disk drive, a disk drive controller with 1-to-1 interleave, a Seagate 40-megabyte (28-ms) hard disk drive, two serial ports, one parallel printer port, and one game controller port. It also includes a 32K-byte RAM cache, a monochrome display adapter

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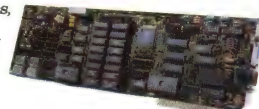
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The unit I tested was equipped with 4 megabytes of RAM and a Maxtor 150-megabyte 5¼-inch ESDI hard disk drive in place of the Seagate unit. Instead of a monochrome display, it had a Paradise VGA Plus 16 board and an NEC MultiSync 2A monitor, and it had a total of 64K bytes of RAM cache. This configuration costs a reasonable \$7495.

I used the Blackship as my primary work computer every day for about six weeks. Most of the time I used the extended RAM and a supplied driver to emulate EMS memory for a disk cache. With the disk cache, it took my Lotus Agenda files, whose category list and heavy disk activity had outgrown my old 80286 system, and made that program useful again. Without the disk cache, though, I had to wait—albeit less than before—for Agenda to respond.

None of the other many application programs I tried failed on the Blackship. It also ran multiple programs using DESQview with no problem. However, the Blackship made its real worth clear while processing numbers and VGA graphics. Two notable examples were drawing MapInfo's detailed maps and plotting the heavens with an obscure astronomy program called EZCosmos. Both programs do calculations and plotting that, on a slower machine, would leave you tapping your fingers.

The unit is a standard desktop design. Inside, the system layout is easy to work with, and I had no trouble accessing peripheral cards. Neither did the system have any trouble working with a CompuCom 8-bit 2400-bps modem card I tried. The Blackship has five 16-bit and two 8-bit slots for add-in cards. It

also has one 32-bit slot for the 32-bit memory card, which was installed in my unit. You can expand the memory to 16 megabytes, although you'll need to buy a daughterboard to exceed 8 megabytes.

The system comes with a one-year parts and labor warranty that's handled exclusively by the manufacturer, so you'll have to send your system back for warranty service. Though not toll-free, the company's customer support is courteous, fast, and competent. When I experienced a problem that turned out to be just an improperly seated drive controller (probably caused by shipping), the company's technical-support staff provided me with solid technical advice.

Overall, the Blackship did an average job on the benchmark tests, and better than some of the big name-brand systems. Considering its reasonable price, it's easy to recommend this computer.

—Dennis Allen

Compaq Deskpro 386/33

Although the Compaq Deskpro 386/33 was not the fastest system tested—either in raw CPU power or in the BYTE cumulative application index—it did score impressive results. Thanks to its 64K-byte cache (with 25-ns static RAM), it was the fourth-fastest system in the BYTE CPU test. In the BYTE application index, it was the fifth-fastest system overall and the fastest system that did not use a special hardware disk cache.

The standard Model 84 comes with 2 megabytes of memory.

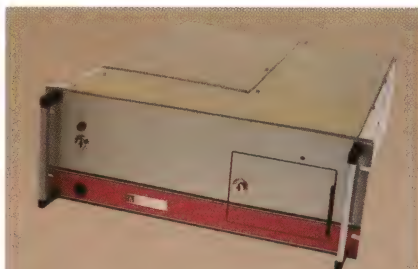
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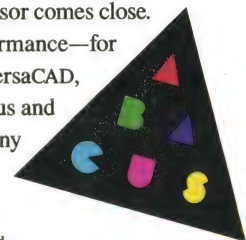


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For additional memory, you must use an expansion board, which fits into a special 32-bit expansion slot. This board has room for seven 2-megabyte memory modules (at a rather hefty \$1299 each), bringing the total memory capacity up to 16 megabytes.

The unit we received had 4 megabytes of RAM, a 33-MHz 80387 math coprocessor, a second 1.44-megabyte 5¼-inch floppy disk drive, a Compaq Advanced Graphics 1024 controller, a Compaq Advanced Graphics color monitor, a Compaq 2400-bps internal modem, a 40-megabyte tape drive, MS-DOS 4.01, and OS/2 1.1. Total price for this system is \$19,657.

In physical appearance, the Compaq system looks like a standard desktop AT clone, considerably larger than the company's other 80386 systems, such as the Deskpro 386/20e. The standard configuration consists of a 1.2-megabyte floppy disk drive, an 84-megabyte hard disk drive, and a VGA controller on the motherboard. One nice touch is the inclusion of a Microsoft-compatible mouse connector on the back panel.

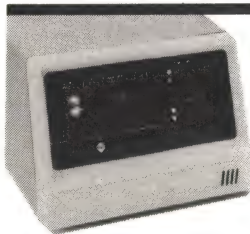
Along with the VGA controller is a VGA pass-through connector. This connector appears to have the same function as the VGA lines on IBM's Micro Channel bus. If you purchase Compaq's Advanced Graphics 1024 board (the company's equivalent to IBM's high-resolution 8514/A controller), the VGA pass-through connector allows the Advanced Graphics board to display high-resolution 1024- by 768-pixel graphics as well as standard VGA graphics.

Like many high-end systems, the Compaq has room for five half-height storage devices. But the Compaq system has one additional feature. On the back panel is a removable grill that allows access to the two rear drive bays. Although Compaq does not spell this out, this possibly could allow all five of the drive bays to be used for removable media, such as floppy disk drives, tape drives, optical drives, or removable magnetic drives. This, along with the system's password protection scheme, indicates that the system could be used well as a file server.

The motherboard seems clean, although I did spot two jumpers. The two sockets that you will most probably need—those for the 80387 and the Weitek 3167 coprocessors—are

continued

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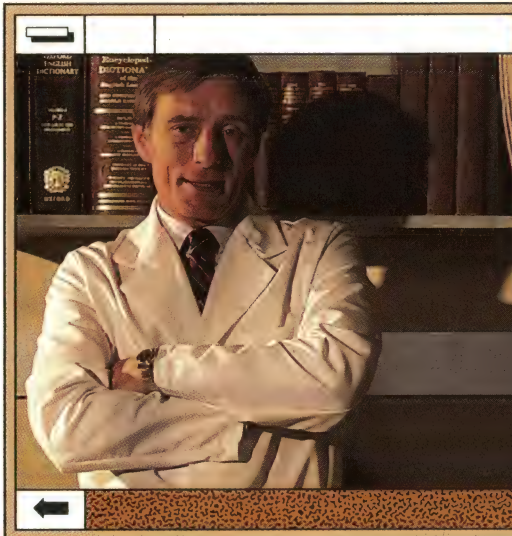


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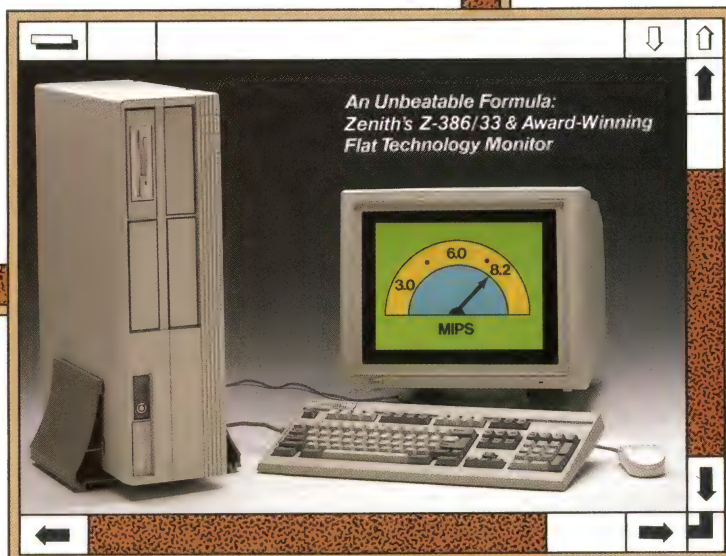
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easy to access. The design may still be in flux, however. Just before the product was announced, the floppy disk drive controller was moved from the motherboard to an expansion card. And although Compaq says that the system's hard disk drive controller is on an expansion card as well, on our system it seemed to be on the motherboard.

Compaq should be commended for a number of small details: for example, the easy way that the system cover can be removed (via two small thumbscrews), the mouse connector on the back panel, and a Setup program that allows you to quickly set the system up. Some things were less than admirable, including Compaq's use of Torx screws inside the system.

The system comes with a one-year warranty. No on-site service or other service contracts are available directly from Compaq.

At a list price of \$10,499 for an 84-megabyte system, the Compaq is surely one of the more expensive systems around. Even with a street price considerably lower, it will still be an expensive system. But Compaq has a reputation for quality, and this system does a lot to uphold that reputation. The high cost of the Deskpro 386/33 should buy a substantial amount of peace of mind.

—Rich Malloy

Dyna Cache 386



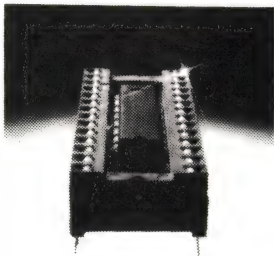
Dyna Computer takes a smorgasbord approach to constructing a 33-MHz 80386; you start with an AMI motherboard and BIOS, and then select from a list of recommended subsystem components. The machine I tested was a sturdy, tower-style unit configured to provide the best performance for under \$10,000. The Dyna Cache 386 was an able performer, coming in sixth in BYTE's cumulative application index.

In addition to a switchable (8- or 33-MHz) 80386 and an 80387, our test machine included 4 megabytes of 70-ns DRAM on the motherboard with room for 4 more megabytes on SIMMs, and up to 8 additional megabytes on a 32-bit add-in

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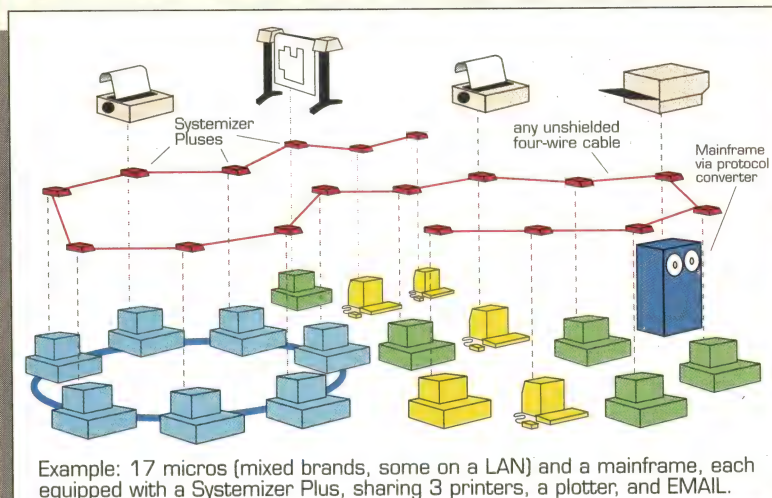
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Altos 386 Series 1000: For Unix Only



Unlike the other machines in this roundup, the Altos 386 Series 1000 does not run MS-DOS except as a guest of the Unix operating system. The Altos does not have an AT bus, a Micro Channel bus, or any other bus, for that matter. It is engineered to run Unix. The AT bus machines are not designed to run a full 32-bit operating system; the Altos machine is.

The 33-MHz Altos has everything except the serial I/O on the motherboard. The basic system comes with eight serial ports, a tape drive, a 40-megabyte SCSI hard disk drive, and 4 megabytes of RAM. Both the CPU data and address buses are 32 bits wide. Performance is further enhanced by a 32K-byte memory cache. You can expand the RAM to 24 megabytes, the hard disk storage to 300 megabytes, and the ports to 24, but all these upgrades require proprietary hardware, which you must buy from Altos.

Unlike with AT-style Unix computers, the Altos's console, as well as any terminals, are connected to serial ports. Typical of all the newer Altos boxes, the machine stands on end and slips under a desk. All ports and switches are on the back. Only the floppy disk drive and tape drive are on the front.

The Altos falls into the category of general-purpose Unix engine. It is not your lightweight AT-bus machine, nor is it the heavy-duty mainframe serving

hundreds of users. It will serve an office or department well. When our Unix minicomputer failed, the Altos filled in very easily. In fact, it outperformed the five-year-old 68020-based minicomputer on every function, even though you might mistake it for a 20-inch-high dwarf version of the 5-foot minicomputer.

The Altos ran most of the low-level BYTE Unix benchmarks (beta version) at 65 percent to 90 percent of the performance of the Everex Step 386/33 running SCO 386 Xenix, but it excelled in a few areas. It created subprocesses twice as fast as the Everex. But the benchmarks showed the Altos able to read, write, and copy file segments at a phenomenal 10 times the rate of the Everex. If you plan to run database applications, this machine is considerably better than any other 80386 in its class.

Usually we don't focus on operating systems in a hardware roundup, but on Unix machines, the quality of the operating system and compiler is as important as the hardware. Altos Unix is a mix of Unix System V, Berkeley Unix, and Xenix. The entire system is designed to work to the best advantage of both the hardware and the operating system. The disadvantage is that everything is a little bit different than on any other Unix system.

In fact, everything about the Altos is just a little bit different. You can't buy it from your average computer vendor;

card. Cache memory consisted of 64K bytes of 20-ns SRAM. The 16-bit Quadrex VGA board with 256K bytes of shadow RAM made the Dyna Cache one of the fastest machines in the scientific/engineering application benchmark category. The system came with a Mitsubishi Diamond Scan monitor.

Storage devices included a Western Digital ESDI controller supporting 1.2- and 1.44-megabyte TEAC floppy disk drives and a Micropolis 147-megabyte ESDI drive with an average seek time of 18 ms. This combination proved slower than many of the other machines in our low-level disk I/O benchmarks.

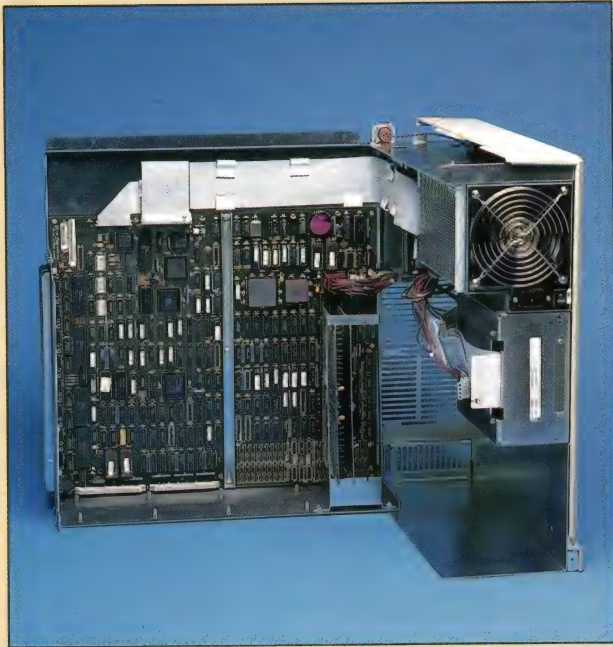
Our test system had one parallel port, one serial port, and a game port on a Courier I/O card (which occupied two card slots), and a second parallel port on the Quadrex card. The backplane had eight slots; one 8-bit, six 16-bit, and one 8-/32-bit. Four of the 16-bit slots were occupied. The system can hold one more full-height or two half-height storage devices.

Compatibility was generally good. The machine worked flawlessly with a variety of add-in cards and application programs. Overall, the Dyna Cache 386 is a well-designed, well-built, and competitively priced machine.

—Rob Mitchell

Everex Step 386/33





you must go to an Altos value-added reseller or a systems house. If you need a good Unix engine for your office and require a generic system, the Altos gives you a lot of performance, and you won't have to find someone other than your vendor to support both the hardware and the operating system. But, as with any proprietary system, you must go totally with Altos or not at all.

—Ben Smith

For raw CPU speed, the Everex Step 386/33 is the fastest PC we've ever tested. Its 6.84 CPU index narrowly beats ALR's 33-MHz machine. On the application side, the Everex didn't fare quite as well; it placed tenth among the 33-MHz PCs. Adding a hardware disk cache would significantly improve its performance.

For \$7599, you get an Everex-designed motherboard, 4 megabytes of 100-ns RAM (expandable to 16 megabytes), an AT-style hard disk drive controller, a 1.2-megabyte 5¼-inch TEAC floppy disk drive, and an adequate 200-W power supply. Our evaluation unit came with 4 megabytes of RAM, a 160-megabyte Control Data hard disk drive and ESDI controller, a 33-MHz 80387 math coprocessor, a Renaissance RVGA II board, and a 14-inch multisync VGA monitor for a total price of \$10,945.

Like all Everex machines, the Step 386/33 is well engineered. The motherboard is free from the wire fixes often found on early-production PCs, and it is housed in a sturdier-than-most stainless steel case. Everex uses a 64K-byte, 20-ns RAM cache of its own design.

Unlike most other 33-MHz PCs, the Step 386/33 provides only one serial and one parallel port. Its eight expansion slots include two 8-bit and six 16-bit slots. All memory mounts on the motherboard, eliminating the need for 32-bit memory-expansion slots. The case can accommodate up to five half-height storage devices. A switch on the front panel allows you to set the operating speed to 8, 16, or 33 MHz.

Though not the least expensive PC in this group, the Everex Step 386/33 is priced reasonably, and its performance speaks for itself. Everex is a midsize PC maker with a solid reputation; buying its 33-MHz PC is a relatively safe choice.

—Michael E. Nadeau

FiveStar 386

FiveStar Electronics' 386 machine comes in two main configurations. The base Model 333 has 1 megabyte of RAM, an Award BIOS, a 1.2-megabyte 5¼-inch (or 1.44-megabyte 3½-inch) floppy disk drive, and an I/O card with serial, parallel, and game ports. The cost is \$3395.

The Model 33/D, which we tested, is built around the same Micronics 09-00021 motherboard but comes with 4 megabytes of RAM, a 90-megabyte Control Data ESDI hard disk drive and controller, DOS 4.0, and an extra serial port and a clock/calendar on the I/O card. The unit also has an 80387 math coprocessor, a FastWrite VGA card driving an NEC MultiSync monitor, and a year's worth of on-site service through General Electric for a total cost of \$8179.

The FiveStar's 33-MHz chip operates at 6, 8, or 33 MHz, selectable by software, or you can select 33- or 8-MHz speeds using a push button/digital readout on the front panel. The 32K-byte, zero-wait-state hardware cache uses the Intel 82385 cache controller. As you can see from the benchmark results, the FiveStar Model 33/D falls about in the middle of the pack on the CPU benchmarks. It led the pack in the FPU tests, but here the differences between systems were minor.

The Micronics motherboard provides five 16-bit AT slots (two of which, in our system, were taken up by the disk and video controllers), two 8-bit slots (one of ours contained the serial/parallel/clock/calendar half-card), and a proprietary 32-bit slot for system memory.

The hard disk is driven by the Distributed Processing Technology (DPT) SmartCache controller for ESDI drives, which

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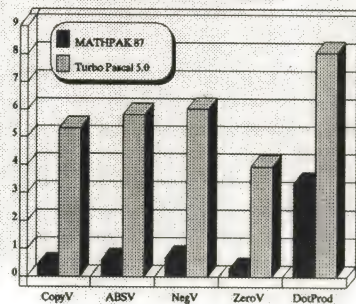
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comes with 512K bytes of RAM on-board. The SmartCache's usefulness is attested to by the Model 33/D's excellent performance in the disk I/O benchmarks.

The video card in the Model 33/D is a FastWrite VGA card from Video Seven. This too has 512K bytes of on-board RAM. The memory card in our unit contained 4 megabytes of system RAM in 80-ns DRAMs. The system can hold up to 8 megabytes on the memory board, or up to 16 megabytes with an optional 8-megabyte daughtercard.

Opening up the case, we found the FiveStar to be a nice, cleanly designed machine, with room for four more mass storage devices. According to its manual, the FiveStar comes with a one-year warranty on materials and workmanship. The company maintains a toll-free number for service.

The cost of the FiveStar is about what you'd pay for a similarly equipped system from many of the other vendors. If your applications tend to be disk-intensive, the ESDI drive and SmartCache combination might make this the system for you.

—Ken Sheldon

Matrix MDP 386-33

The MDP 386-33 features a Micronics motherboard in a tower enclosure. It is an AT compatible with five 16-bit, two 8-bit, and one dedicated memory slot. The speed of the I/O bus is hardware-switch-selectable between 8.1 and 11 MHz. In its basic configuration, the MDP 386-33 has two serial ports, a parallel port, a game port, and a DTC 7280 hard/floppy disk drive controller with a 1.2-megabyte floppy disk drive. It also has 4 megabytes of DRAM and 32K bytes of static RAM (SRAM) for the memory cache.

The interior layout makes it easy to configure and upgrade the machine. The I/O slots, configuration DIP switches and jumpers, 80387 socket, and sockets for added cache memory are easily accessible. The motherboard is free of visible jumpers. The machine I tested came with a Phoenix BIOS ROM; an Award BIOS ROM is also available. I encountered no hardware or software compatibility problems.

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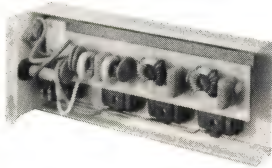
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The one problem I found with the design of the machine involves the memory slot. Either the alignment of the slot with the mounting bracket is off or the slot is too close to the bracket, because the memory card is bent slightly. This didn't affect the operation of the machine for the three weeks I used it, but the stress that the bend creates could cause long-term problems with the sockets for the memory chips.

To keep the bottleneck between the processor and memory as free as possible, the system uses a 32K-byte direct map or two-way set-associative memory cache (hardware-selectable). The cache consists of 25-ns SRAM chips that provide zero-wait-state performance. The cache hit rate is about 96 percent. On a cache miss, the system accesses the 80-ns DRAMs that form the main memory. This memory access entails two wait states. Both the SRAM on the motherboard and the DRAM in the memory slot run at 33 MHz.

The SRAM cache is upgradable to 64K bytes; the added 32K bytes brings the hit rate up another percentage point. Main memory is expandable to 8 megabytes on the memory board, and to 16 megabytes using a daughterboard.

With a CPU index of 5.75, the Matrix MDP 386-33 finished (albeit barely) in the top half of its class—an excellent showing considering its price. The problem with the Matrix machine, and the reason it brought up the rear in the application benchmarks, is its disk subsystem. The controller uses an ST-506 interface—a good ST-506, to be sure, but an ST-506 nonetheless. Using this interface in a 33-MHz machine is nearly criminal, as the disk and application benchmarks show. A high-powered machine needs a fast disk interface. Matrix supplies optional ESDI interfaces; it should make them standard.

One application area where the Matrix machine excelled is the scientific/engineering benchmarks. The review unit came with a high-resolution, 16-bit, PaeLIT VGA board which, in conjunction with the machine's very good CPU and FPU performance, made the MDP 386-33 a tempting choice (\$7190 with the VGA board and 72-megabyte hard disk drive) as a CAD workstation.

Buying a Matrix MDP 386-33 won't give you that warm, fuzzy feeling you might get with a Compaq, but it can save you money—even after you shell out the extra \$1425 for the 145-megabyte ESDI disk upgrade option. Don't use it as a file server on large networks, but do consider it for less-disk-intensive applications.

—Bob Ryan

Micro Express ME 386-33

Distinguishing itself from some of the 33-MHz pack, Micro Express provides a caching disk drive controller in the ME 386-33 to help it avoid I/O bottlenecks. The controller, which is included in the base system price, helped place the ME 386-33 among the top I/O performers. Depending on the hard disk drive used, you can choose either an ESDI or an ST-506 DPT controller, each providing 1-to-1 interleaving and 512K bytes of on-board memory.

The BYTE benchmark tests ranked the Micro Express third fastest in disk speed, while its CPU speed placed a modest eleventh. But the controller helped the ME 386-33 to perform respectably in the database, scientific/engineering, and compiler application tests. Notably, the system scored second overall in cumulative application performance.

However, even though our evaluation unit used a 150-megabyte ESDI hard disk drive, the controller recognized only 133 megabytes of formatted space. The company says the controller

continued

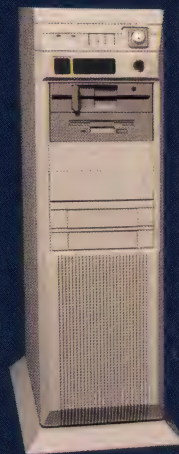
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doesn't acknowledge disk space above 1024 cylinders in DOS, idling the remaining 17 megabytes. But Micro Express claims that DPT has developed an extended BIOS that will plug into an existing controller socket and allow use of the full disk space. Micro Express plans to offer the extended BIOS as a standard component with future ME 386-33 systems.

In other respects, the ME 386-33 sports a clean and typical design. Its American Megatrends, Inc. (AMI) motherboard is uncluttered and allows for eight expansion boards to be installed in one 8-bit, one 32-bit, and six 16-bit compartments.

A standard 4 megabytes of RAM comes with the machine. Eight logic chips provide a 64K-byte 20-ns static cache. Memory can be expanded to 8 megabytes on the main board or to 16 megabytes with an expansion board. The motherboard also includes four SIMM sockets. The system accepts either an Intel 80387 or a Weitek math coprocessor chip.

A 15-month repair warranty covers parts and labor. The company also provides a telephone service that allows customers to call technicians about machine problems. In some cases, you can arrange to have replacement boards sent or, if necessary, ship the entire computer back to the company for service.

The base ME 386-33 sells for \$5995 and includes either a 1.2-megabyte 5¼-inch or a 1.44-megabyte 3½-inch floppy disk drive, one parallel and two serial ports, and a 101-key keyboard. Our evaluation system had a 150-megabyte ESDI hard disk drive (\$1500), a VGA Plus card and an NEC MultiSync 2A monitor (\$750), an 80387 math coprocessor (\$750), and two floppy disk drives. At \$9125, this system demands less than two dollar for near-high-end performance.

—Alan Joch

National MicroSystems Flash 386-33

The Flash 386-33 would make its comic-book namesake proud. Built around a 33-MHz Micronics motherboard and a DPT high-speed caching disk controller, the unit turned in exceptional benchmark times—often outrunning the bigger-name systems. The base price for the Flash 386-33, which includes 4 megabytes of memory, a disk drive controller, a floppy disk

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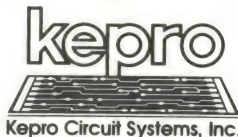
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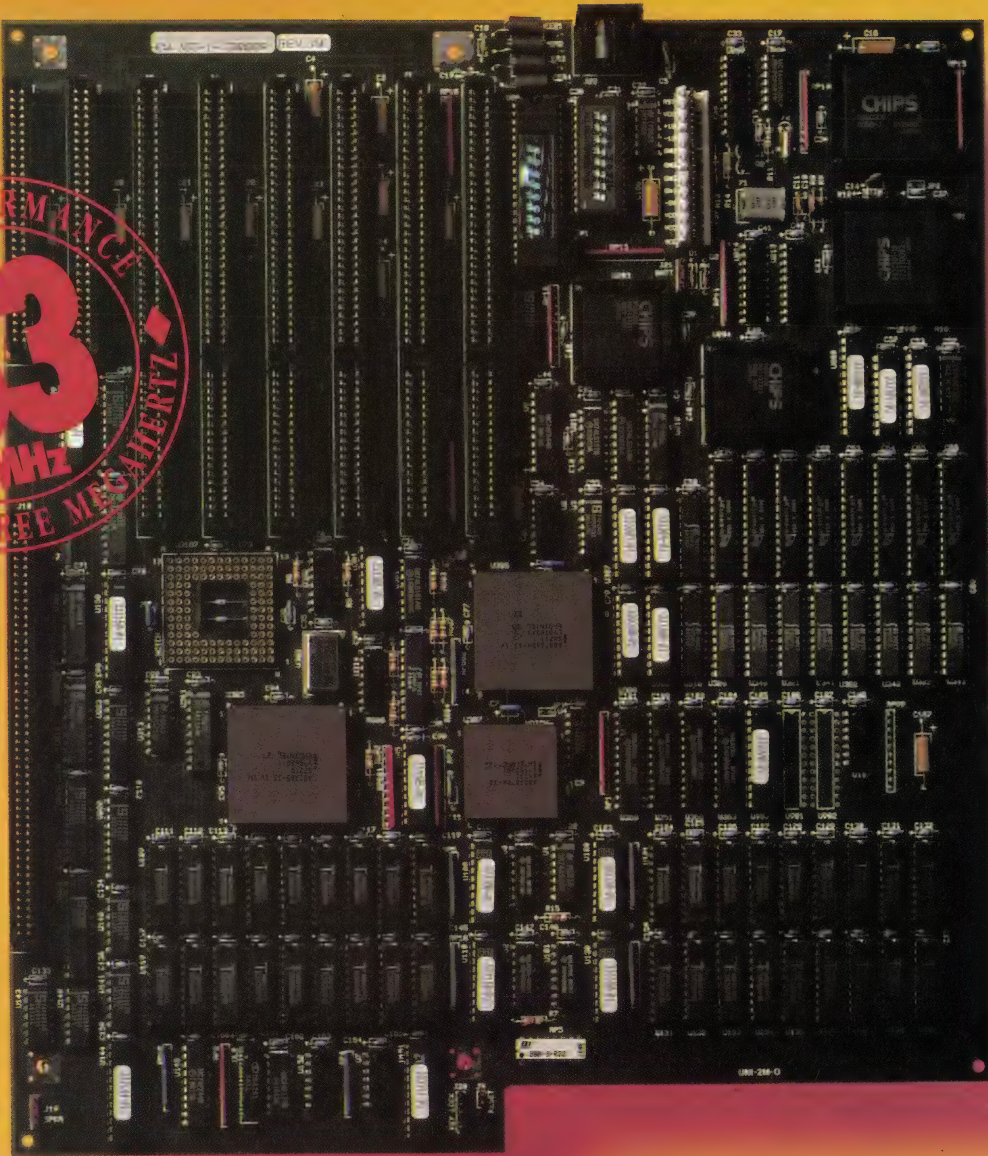
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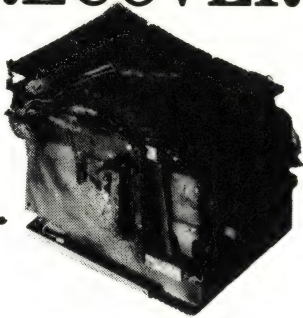
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drive, a 200-W power supply, and a keyboard, is \$4999. With the hard disk drive, VGA video system, and math coprocessor that our review unit had, the complete system rings up at \$7995.

The Micronics design puts all system memory on a daughter-card that fits in a proprietary 32-bit slot. Total 32-bit memory capacity, which will require a piggyback unit in addition to the daughterboard, runs up to 16 megabytes. The unit we tested had a daughterboard half-filled with 80-ns, 1-megabit DRAM, bringing the system RAM to 4 megabytes. A 33-MHz Intel 82385 manages the 25-ns, 64K-byte static cache.

The CPU memory subsystem performed admirably on our low-level benchmarks, placing the Flash 386-33 solidly alongside Compaq's entry. CPU performance also contributed to the Flash 386-33's strong showing on our application tests.

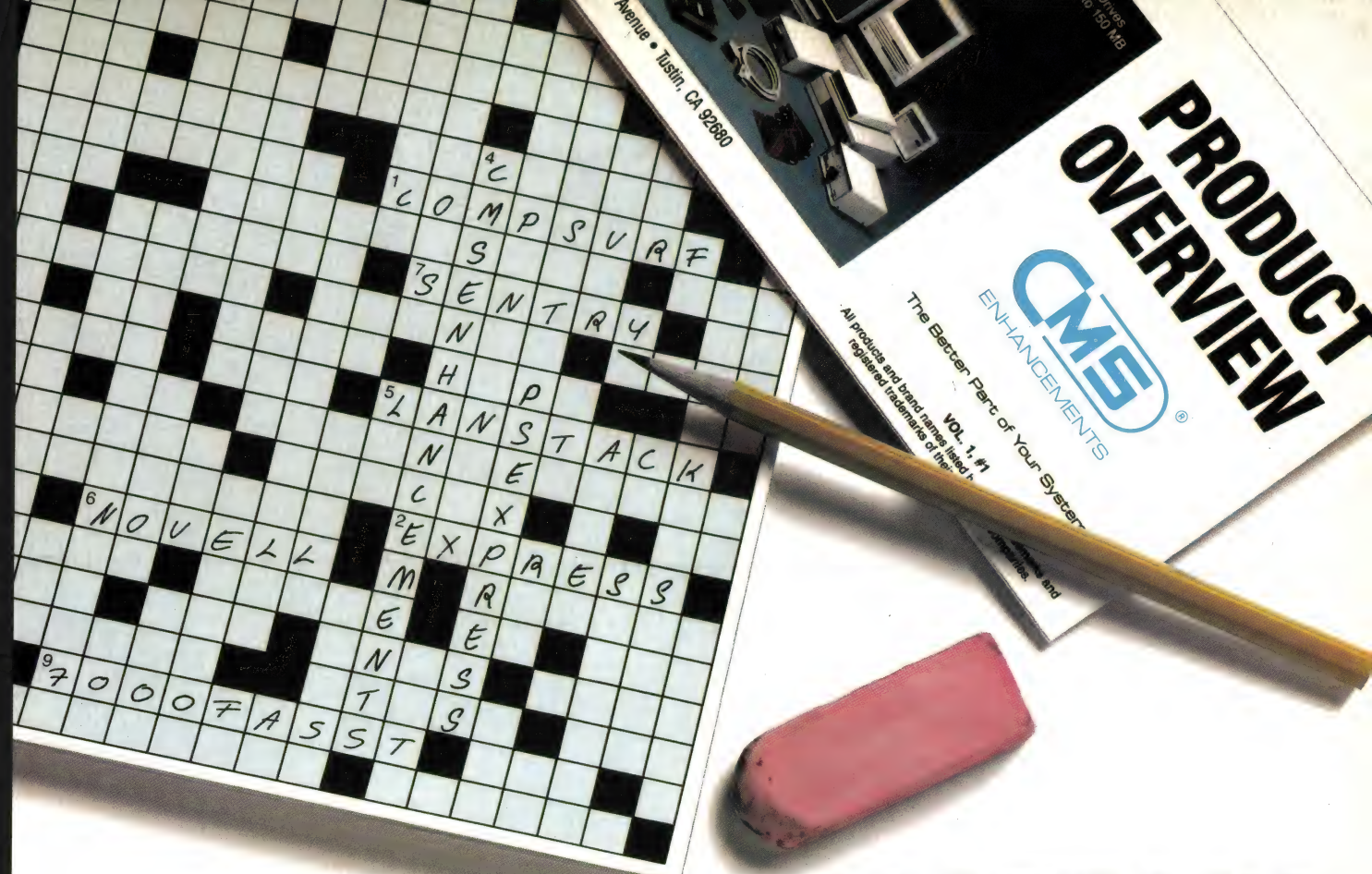
Other system board features include a DIP switch-selectable bus speed of 8.25 or 11 MHz, five 16-bit and two 8-bit slots, a Phoenix ROM BIOS, and 80387 support. The unit can also run a Weitek 3167 with an adapter card. Since high bus speeds often mean compatibility problems, we ran all our benchmarks at the default 8.25-MHz bus speed.

Disk I/O performance was another key in the Flash 386-33's outstanding application index. The hard disk drive unit is a 150-megabyte Control Data ESDI drive (standard type formatting under DOS will leave you with 127 megabytes) with a respectable 18-ms average access time. National Microsystems' standard 33-MHz configuration also includes DPT's SmartCache disk controller, outfitted with 512K bytes of RAM. Low-level disk benchmarks best illustrate the dramatic effect of the SmartCache—systems with the controller (the SIA 386/33, the Micro Express ME 386-33, and the Flash 386-33) all had disk I/O indexes higher than 6, while noncached units typically scored in the mid-2's. If you plan to use the Flash 386-33 as a file server and need really screaming disk performance, you can add cache memory to the controller up to a ceiling of 16 megabytes.

Peripherals such as a reasonably comfortable Chicony keyboard and a Sony VGA monitor round out the Flash 386-33. Video speed was disappointing, but the Sony monitor is easy on the eyes and provides good contrast.

—Steve Apiki

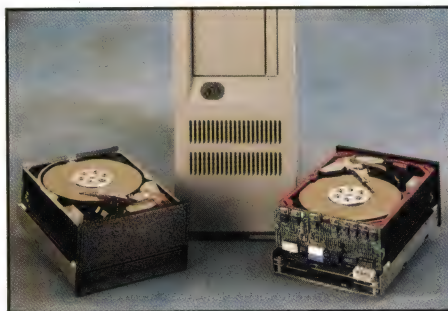
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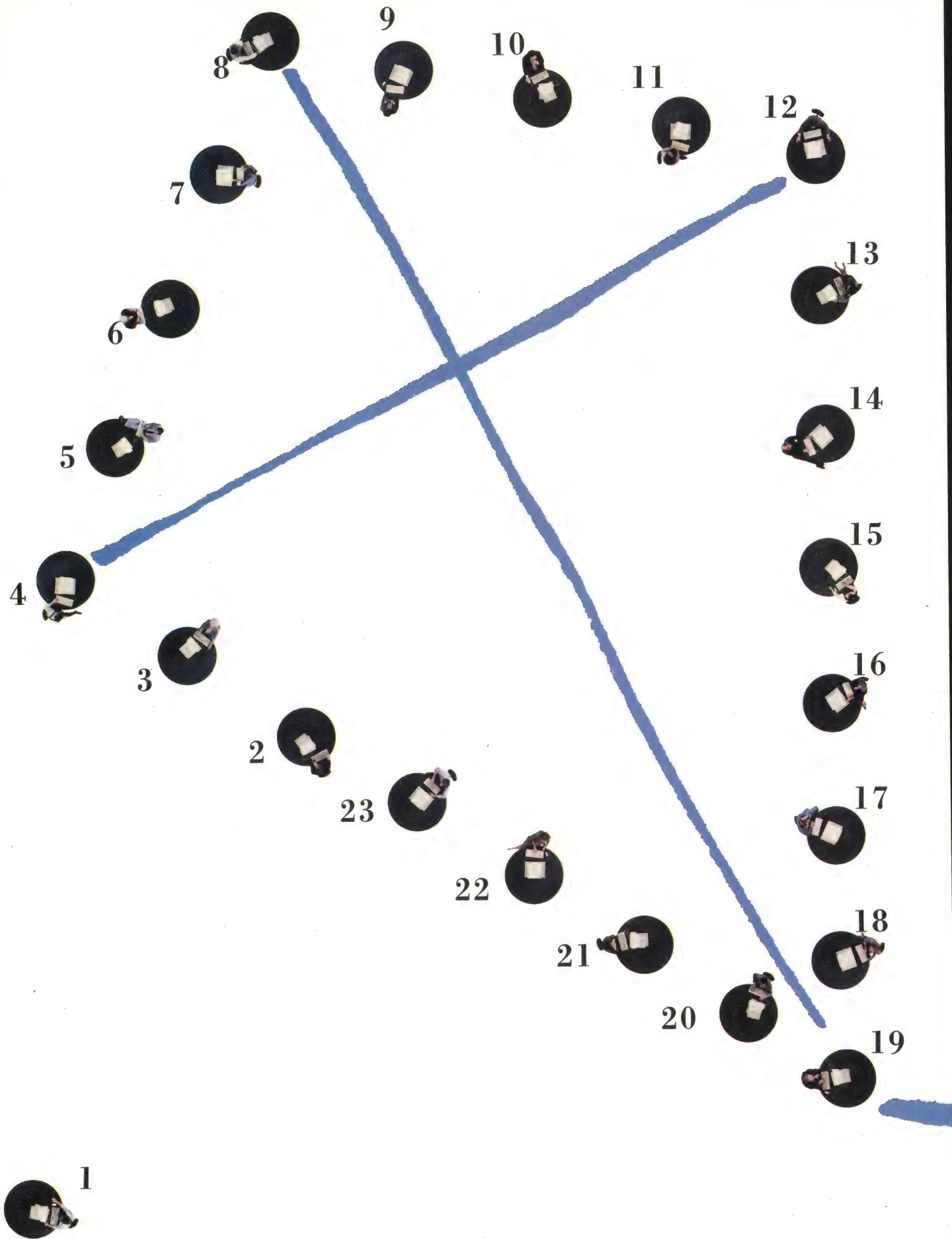


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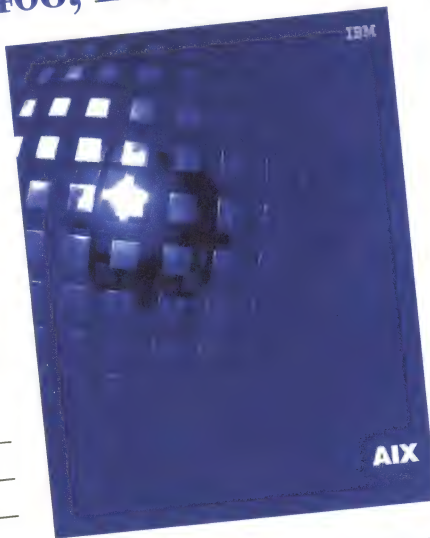
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PC Link 386/33



I doubt that any of the other 33-MHz machines got the same strenuous workout as the PC Link 386/33. As soon as it arrived, I set it up in the BYTE Lab. Immediately, the hard disk drive and the open card slots began to fill up. In addition to the standard BYTE application benchmarks, the PC Link transferred megabytes of data using Lap-Link and a Bernoulli Box; ran at least three versions of Windows; tested a new 400-dot-per-inch

laser printer using Micrografx Designer 2.0; accessed BIX, Prodigy, and BYTE's editorial LAN; ran DESQview 386, Norton Utilities 4.05, and Scanning Gallery with an HP ScanJet; and negotiated the numerous small chores expected of all our lab computers. The PC Link was up to the task. It ran everything from PageMaker 3.0 to a new desktop publishing software package currently in beta testing. The only hitch was an annoying mechanical problem with the 3½-inch floppy disk drive.

PC Link Corp. sells the 33-MHz system in two basic flavors. Both models are based on the Hauppauge 386 Motherboard/33 and come with 4 megabytes of RAM, a 101-key Enhanced keyboard, a 220-W power supply, one parallel and one serial port, a 1.2-megabyte floppy disk drive, and a 16-bit Trident VGA board. Only the disk drive type distinguishes the configurations: The Model 160 (\$5995) supports a 159-megabyte, 17-ms ESDI Micropolis hard disk drive, and the Model 330 (\$6995) packs a 330-megabyte, 18-ms ESDI Micropolis drive.

Our evaluation unit was the Model 160 with the following options: a 1.44-megabyte 3½-inch floppy disk drive, a 33-MHz 80387 math coprocessor, a Video Seven 16-bit VGA adapter, and an NEC MultiSync 3D monitor, for a total of \$7818.

Three of the system's expansion slots are occupied, leaving four 16-bit slots free. An eighth expansion slot supports a dedicated 32-bit memory bus. A monitor is not included with any model.

The Intel CPU can access up to 64 megabytes of 32-bit memory. The motherboard comes stuffed with 4 megabytes of 80-ns RAM; further memory upgrades require a card for the dedicated 32-bit memory slot. The PC Link optimizes memory access with a 64K-byte 20-ns cache and four banks of interleaved DRAM. Extended memory conforms to EMS 4.0 specifications. The motherboard also supports either an 80387-33 or a Weitek 3167-33 math coprocessor.

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The PC Link did not excel on the BYTE benchmarks, but it performed credibly for an inexpensive, no-frills system. Many of the systems reviewed here boost their performance with expensive disk controllers and on-board caches. The PC Link, on the other hand, offers only a disk-cache utility on the bundled disk. A software cache is not as efficient as a hardware one, and it also consumes valuable RAM. The decision to forego an on-board cache may stunt the benchmark results, but such choices also keep a rein on the system's price. PC Link has done a good job balancing the price/performance equation. Nothing spectacular, perhaps, but a solid machine at a reasonable price.

—Stanford Diehl

SIA 386/33



After the BYTE Lab tested Systems Integration Associates' 386/33, we realized how hard-disk caching can influence system performance. With an optional 4.5 megabytes of disk-cache memory, the SIA 386/33 achieved the BYTE Lab's rating as one of the fastest PCs on the market.

A caching controller from DPT is one key; it allows the SIA 386/33 to read and write to the controller cache while the controller card simultaneously accesses the disk. Because of the DPT controller, the SIA 386/33 blasted its nearest 33-MHz competitor by 18 percent on the cumulative application index. And the disk caching can be expanded to 12 megabytes.

CAD redraws were, at most, a nuisance for this machine. Word processing disk-access applications were even less taxing.

To keep main (motherboard) memory from slowing down the processor, all SIA 33-MHz systems include a 64K-byte, direct-mapped, 20-ns SRAM cache. SIA claims zero-wait-state operation and an 81 percent hit rate for the write-through cache, operated by a discrete logic controller. In a direct-mapped design, each memory access involves comparing a tag (which specifies blocks within the cache) with part of the requested address. The system uses faster 15-ns SRAM to store the frequently used cache tag. Up to 16 megabytes of main memory can be cached; accessing any memory installed beyond this limit will slow the system considerably.

The SIA 386/33 ships with 4 megabytes of 70-ns DRAM. Four banks for DIP memory are available on the motherboard, along with four SIMM slots. DIP sockets are compatible with both 256K-byte and 1-megabyte DRAM chips. SIA says that

both SIMM and DIP sockets are compatible with the 4-megabyte versions of each package.

With 1-megabyte parts, you can get up to 8 megabytes on the motherboard; when 4-megabyte components are released, the board will take not 32, but 16 megabytes—a system board limit imposed by the AMI BIOS.

The 10-bay tower is well designed, with cabling connections up top where they're protected by a slide-off cover. The cover has handholds for moving the 75-pound behemoth. Loosen two screws, slide the cover off, and you have easy access to install drives and cards in the swing-mounted side cover.

You can easily distinguish the 10-bay system from the others from the loud roar of the two thermostatically controlled cooling fans that drag filtered air past the 350-W power supply. The standard configuration (\$6490) has a PS/2-style keyboard, 4 megabytes of RAM, one serial port, and one parallel port. It does not have any hard disk drives or a caching controller.

The machine I reviewed had a second 1.2-megabyte floppy disk drive, an 80387 math coprocessor, an extra serial port, a 16-bit VGA card and VGA color monitor, two 16.5-ms, 680-megabyte hard disk drives with an accompanying DPT caching controller, a 125-megabyte tape drive, and a DPT mirroring kit. The total cost for this system is a whopping \$26,365.

As configured, this machine is designed for heavy-duty file server applications for large LANs. The mirroring kit works with the two hard disk drives, mirroring the information from one onto another for backup. Besides transparently writing on a second hard disk drive, the SmartCache mirroring kit automatically patches bad sectors with good data from the mirrored drive. Like the mirroring, which is handled transparently by the controller, patching sectors is transparent. —Roger Adams

Tangent 333

My first impression of the Tangent 333 was that you could live in this box. The huge tower measures almost 2 feet deep, just as high, and 9 inches wide; there's enough space inside for 10 half-height mass storage devices.

Even though the unit I tested had two floppy disk drives and a 100-megabyte hard disk drive (all ESDI), and I/O boards that included a Video Seven FastWrite VGA card, a multiport I/O card (with two serial, one parallel, and one game port), plus the controller board for the disk drives, the insides looked empty and lonely. Like Dyna, Tangent builds its systems to each customer's specifications; it offers no standard models. The price of the system I used was \$6995.

This is a system you won't easily outgrow. The power supply is a large two-fan cube mounted in the bottom of the case. Regulated by a temperature sensing circuit, both fans blow air up and across a Mylex motherboard mounted so that the I/O boards are installed with their backsides pointing up.

This means that you attach monitor cables, keyboard cables, and whatnot across the top. But don't worry about spilling coffee into your RS-232C connector—a special cowl covers the top of the machine, protecting its insides like a chimney hat.

The power supply in the model I tested was rated at 250 W continuous, but if you're certain to be loading your machine up, Tangent sells models with supplies rated at 360 W.

The motherboard appears to be capable of handling anything you can throw at it. It accepts either a 33-MHz 80387—which was in the system I tested—or a Weitek 3167 coprocessor. The peripheral board slot arrangement is geared to versatility: four 16-bit slots, an 8-bit slot, and two Intel AT/32-bit slots. If your

continued



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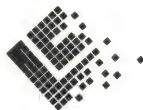
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8-bit boards are fast enough, they'll run fine in the 16-bit slots; conversely, a 16-bit card works in the AT/32-bit slots.

A proprietary slot holds the main memory board. The only memory on the motherboard is 128K bytes of 25-ns SRAM. The machine I tested housed 4 megabytes of conventional DRAM, but Tangent said that the Mylex memory board could handle 4-megabit SIMMs (expected in the next six months), which would be able to take the machine up to 32 megabytes.

Memory is arranged on the board in interleaved fashion; there are two banks, and the system refreshes one bank while the CPU accesses the other. My machine had only one bank populated, so the system was unable to perform this clever refresh interleaving. Consequently, Tangent claims, the system suffers a 2 percent to 3 percent performance degradation.

The entire front of the machine is a door that swings open to expose the power switches and hard disk drive. (Floppy disk drives are accessible through a cutout, even when the door is closed.) You can lock this door, and when you do, no one can get at the screws that loosen the side panel for access to the internals. Neither are the top cowling screws accessible; it's difficult for someone to tamper with the I/O port cables.

The Tangent system turned in mediocre performance on our benchmarks, but this doesn't dampen my enthusiasm for it. The Tangent should make an ideal network server or Unix machine. With plenty of room for expansion, an eye toward tamper-resistance, and a well-designed power system, this is hardware you won't have to worry about. —Rick Grehan

Zenith Z-386/33

Several features of the Z-386/33 make it stand out. All the data lines to the serial and parallel ports have RF filters to minimize radio frequency interference; the system has FCC Class B approval. A built-in Monitor program allows you to diagnose, set up the computer, and do programming. A lithium "Smart Battery" circuit displays an error message telling you to replace the battery before you lose the setup information in CMOS RAM. Finally, the Zenith documentation is excellent. It is well written, well organized, and liberally illustrated.

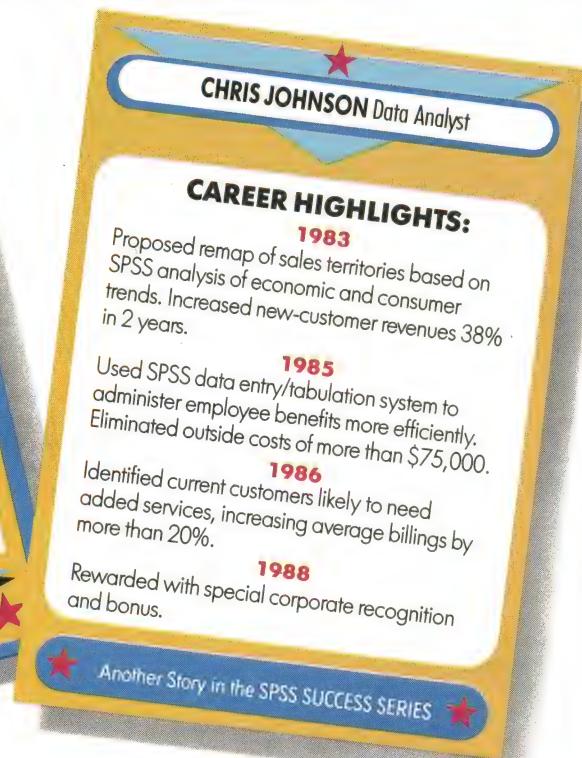
The Zenith Z-386/33 came configured with one 1.44-megabyte 3½-inch floppy disk drive, a 155-megabyte MiniScribe

continued

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March 14, 1989



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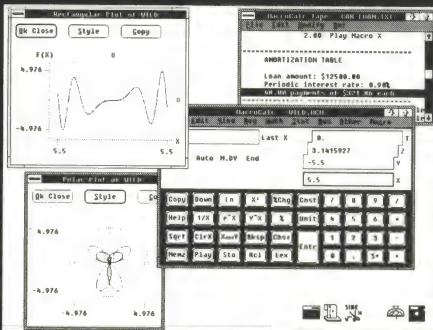
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3180E ESDI hard disk drive, 3 megabytes of 80-/100-ns system RAM, 16K bytes of 15-ns SRAM for the cache, and a 200-W power supply. It also came paired with the Zenith ZCM-1490 Flat Technology 14-inch analog color monitor. The system comes with MS-DOS 3.3 Plus and Windows/386. The total price of this system is \$13,197.

The Z-386/33 has seven expansion slots on the motherboard. Three are for standard, 16-bit, AT-compatible cards. The other four are Zenith's proprietary 32-bit SuperSet slots that are compatible with 16-bit cards and with Zenith's 32-bit memory-expansion and I/O cards.

The computer is unusual because the motherboard holds the system RAM, CPU, FPU (80387 or Weitek 3167), cache RAM, and expansion slots. The Zenith BIOS and Monitor program ROMs, real-time clock circuit and battery, serial and parallel ports, and additional support circuits are on the I/O card that plugs into one of the 32-bit expansion slots.

Eight slots are available for the system memory. Either 1- or 4-megabyte SIMMs can be installed for a maximum of 8 or 32 megabytes of RAM on the motherboard. Optional Zenith ZA-3600-MQ memory-expansion cards can be plugged into the 32-bit slots to increase system RAM to a total of 64 megabytes.

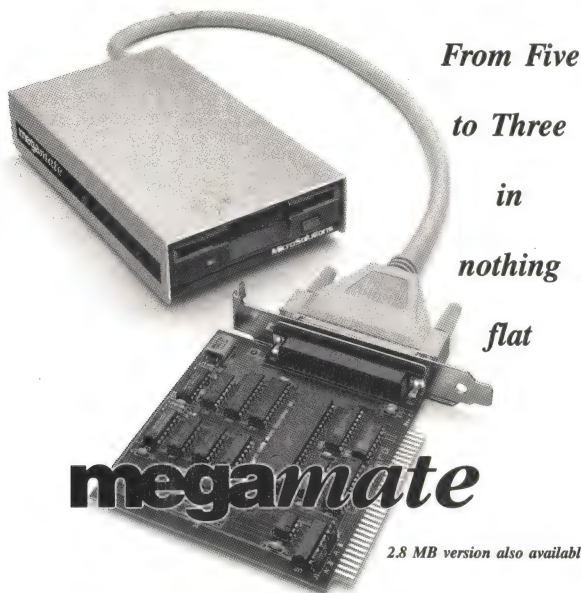
The 16K bytes of RAM for the cache is located on a separate card that plugs into its own slot on the motherboard. Zenith anticipates offering a 256K-byte cache card in the future.

There is space for four half-height devices in the front panel. The floppy and hard disk drives are mounted in cradles. Remove one screw, and the cradle that holds two drives can be easily moved back and lifted out of the chassis.

The floppy and hard disk drives are controlled by a Data Technology ESDI hard/floppy disk drive controller card. Zenith gives it a data transfer rating of 10 megabits per second with a 1-to-1 disk interleave.

The hard disk drive versions of the Z-386/33 come with a Z-549 VGA card made by Sigma Designs. On boot-up, the video BIOS ROM is copied to 32-bit RAM to improve performance. The card provided a crisp display on the Zenith monitor.

The Zenith Z-386/33 is not at the top of the list when it comes to performance—perhaps because it is keeping such exotic company in this review. Where the Zenith does shine is in the overall quality of its design and construction.—Stan Wszola ■



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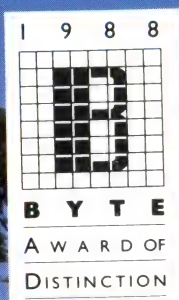
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Benchmarks at a Glance: 1989

*BYTE's performance rankings
of popular IBM PC compatibles and Macs*

Compiled by Stanford Diehl



Ever since the new BYTE benchmarks debuted in June 1988, a diverse field of microcomputer systems has vied for the title of "fastest personal computer." The BYTE Lab has busily tested the gamut of systems from 33-MHz network servers to the new notebook-size laptops. The boxes keep shrinking while the power within keeps growing, and new speed champions appear almost daily. Still, some systems deserve special notice.

While the crop of 33-MHz machines now dominates the top of our list, the ALR FlexCache 25386 clung to the top spot for over six months. At one time, a slick memory-caching scheme was enough to lead the pack. But now, with most observers agreeing that 80386 speeds have topped out, vendors are using more extreme measures to keep ahead, using extensive caching and top-of-the-line components in their speed demons.

As the BYTE benchmarks have evolved, so have the available computer systems. The Compaq Deskpro 386/16, still a powerful desktop model, has dropped to the bottom tier. The portables are now formidable foes, seriously competing with full-fledged systems. The Toshiba T5200 is one of the top 20-MHz performers, and the IBM PS/2 Model P70 edged out the PS/2 Model 70-121. The day of the desktop portable has arrived.

The 80386SX machines are also gaining stature. They, too, achieve a respectable showing on our list, comparing favorably with the 80386/16 machines. If the SX prices drop a little further, the chip may become significant after all.

As always, the BYTE benchmarks offer a glimpse of low-level component performance as well as application-specific performance. You can easily evaluate each system's overall standing, or you can analyze a system's performance by one of four component modules or one of five separate applications. The listing also tells you when each machine was reviewed or otherwise mentioned in the pages of BYTE if you'd like a more detailed picture of a system.

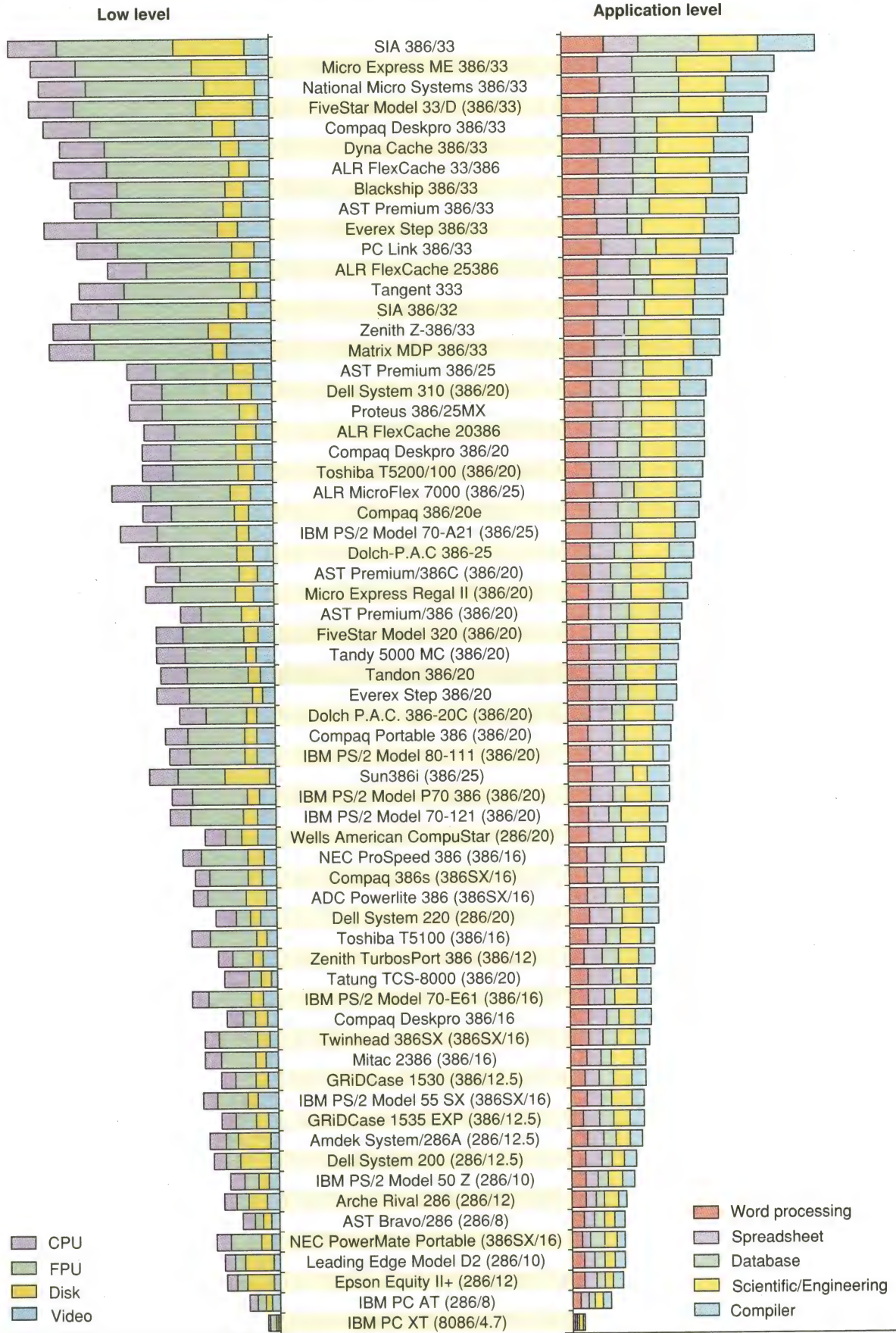
The BYTE benchmark indexes are relative. The IBM
continued

BYTE BENCHMARK INDEXES—WITH MATH COPROCESSOR

Computer	Month appeared	Low-level				Applications					Cum. appl. indx.
		CPU	FPU	Disk	Video	WP	SS	DB	Sci./ Eng.	Cmplr.	
SIA 386/33	IBM Spcl. 89	6.27	14.97	8.99	3.27	5.49	4.32	8.09	7.42	7.32	32.64
Micro Express ME 386/33	IBM Spcl. 89	5.66	15.06	7.02	2.97	4.76	4.32	5.83	7.12	5.55	27.58
National Micro Systems 386/33	IBM Spcl. 89	6.06	15.07	6.48	2.01	5.08	4.35	5.77	6.00	5.37	26.58
FiveStar Model 33/D (386/33)	IBM Spcl. 89	5.74	15.75	7.14	2.22	4.82	4.31	5.91	5.90	5.53	26.47
Compaq Deskpro 386/33	IBM Spcl. 89	6.09	15.50	2.90	4.53	4.28	5.01	3.00	7.86	4.46	24.61
Dyna Cache 386/33	IBM Spcl. 89	5.67	14.86	2.56	3.85	5.02	4.27	2.91	7.51	4.42	24.13
ALR FlexCache 33/386	IBM Spcl. 89	6.74	15.66	2.60	2.83	4.61	4.50	2.88	7.18	4.86	24.02
Blackship 386/33	IBM Spcl. 89	6.03	13.71	2.37	3.61	4.69	4.45	2.89	7.30	4.44	23.77
AST Premium 386/33	IBM Spcl. 89	4.80	14.21	2.32	3.89	4.11	4.22	3.01	7.23	4.11	22.69
Everex Step 386/33	IBM Spcl. 89	6.84	15.48	2.45	4.26	4.43	3.93	1.96	8.05	4.25	22.62
PC Link 386/33	IBM Spcl. 89	5.10	14.87	2.83	2.11	5.03	4.43	2.68	5.51	4.36	22.01
ALR FlexCache 25386	Nov. 88	5.07	10.55	2.74	2.57	4.41	4.13	2.83	5.80	4.08	21.24
Tangent 333	IBM Spcl. 89	5.73	14.83	2.28	1.79	4.57	4.45	2.45	5.43	4.27	21.17
SIA 386/32	Apr. 89	5.99	14.20	2.36	3.06	4.41	4.07	2.02	6.24	3.94	20.67
Zenith Z-386/33	IBM Spcl. 89	4.79	15.10	2.96	5.05	3.91	3.97	1.87	6.59	3.85	20.19
Matrix MDP 386/33	IBM Spcl. 89	5.75	15.07	1.93	5.73	3.95	3.90	1.74	7.09	3.43	20.11
AST Premium 386/25*		3.78	9.92	2.49	2.34	3.62	3.93	2.60	5.36	3.68	19.20
Dell System 310 (386/20)	Oct. 88	3.91	8.38	3.21	2.45	3.45	3.56	2.84	4.98	3.41	18.24
Proteus 386/25MX*		4.26	9.97	2.37	1.72	3.69	3.88	2.40	4.33	3.66	17.95
ALR FlexCache 20386	Jun. 88	3.92	7.93	2.50	2.01	3.44	3.51	2.88	4.66	3.44	17.94
Compaq Deskpro 386/20	Feb. 88	3.61	8.34	2.23	2.54	3.20	3.51	3.09	4.67	3.45	17.93
Toshiba T5200/100 (386/20)	Aug. 89	3.96	8.27	2.22	2.16	3.34	3.66	2.57	4.89	3.40	17.86
ALR MicroFlex 7000 (386/25)	Sep. 89	4.99	10.29	2.41	2.97	3.54	3.82	1.50	5.45	3.30	17.61
Compaq 386/20e*		3.62	8.19	1.89	3.03	3.26	3.64	2.62	4.68	3.07	17.26
IBM PS/2 Model 70-A21 (386/25)	Jul. 89	4.71	10.23	1.64	2.96	3.42	3.75	1.52	5.33	2.62	16.64
Dolch-P.A.C. 386-25	Aug. 89	3.84	8.77	2.12	2.64	3.16	3.14	2.37	4.67	3.11	16.45
AST Premium/386C (386/20)*		3.26	7.42	2.31	2.28	3.12	2.60	2.61	4.50	3.31	16.14
Micro Express Regal II (386/20)	Aug. 89	3.30	8.08	2.51	2.50	2.93	3.18	2.22	4.29	3.14	15.76
AST Premium/386 (386/20)	Sep. 88	2.51	5.26	2.41	1.90	2.80	2.90	2.42	3.98	2.74	14.85
FiveStar Model 320 (386/20)	Jun. 89	3.31	7.99	1.66	2.11	3.07	3.21	1.49	4.31	2.59	14.67
Tandy 5000 MC (386/20)	Feb. 89	3.71	7.91	1.25	2.26	2.97	3.23	1.50	4.35	2.23	14.27
Tandon 386/20	Jun. 89	3.30	8.02	1.49	1.71	2.91	3.19	1.52	3.97	2.41	14.01
Everex Step 386/20	Aug. 88	4.11	8.14	1.41	1.59	2.94	3.37	1.55	3.67	2.46	13.98
Dolch P.A.C. 386-20C (386/20)	Jan. 89	3.30	5.35	1.41	2.23	2.96	2.78	1.68	3.79	2.37	13.58
Compaq Portable 386 (386/20)	Aug. 89	2.82	7.34	1.60	2.46	2.68	3.11	1.49	3.73	2.32	13.33
IBM PS/2 Model 80-111 (386/20)	Nov. 87	2.68	6.97	1.53	2.31	2.81	3.07	1.45	3.63	2.21	13.16
Sun386i (386/25)	Dec. 88	3.61	6.02	5.87	0.70	3.24	2.66	2.36	1.94	2.96	13.16
IBM PS/2 Model P70 386 (386/20)	Aug. 89	2.66	6.98	1.62	2.16	2.99	2.88	1.35	3.58	2.22	13.02
IBM PS/2 Model 70-121 (386/20)	Jan. 89	2.66	6.84	1.74	2.34	2.63	2.74	1.46	3.75	2.15	12.72
Wells American CompuStar (286/20)	Apr. 89	2.74	2.04	2.01	2.30	2.62	3.11	1.65	3.06	2.06	12.49
NEC ProSpeed 386 (386/16)	Aug. 89	2.41	6.00	2.15	1.59	2.34	2.33	2.14	3.11	2.37	12.29
Compaq 386s (386SX/16)	Nov. 88	1.86	5.03	1.78	1.87	2.24	2.15	2.06	3.01	2.05	11.51
ADC Powerlite 386 (386SX/16)*		1.92	4.88	2.64	1.37	2.38	2.25	2.48	2.24	2.13	11.47
Dell System 220 (286/20)	Dec. 88	2.72	1.73	1.40	2.02	2.71	2.68	1.39	2.55	2.11	11.44
Toshiba T5100 (386/16)	Aug. 89	2.38	5.90	1.34	1.32	2.25	2.48	1.69	2.64	1.97	11.04
Zenith TurbosPort 386 (386/12)	Aug. 89	1.96	2.36	1.48	1.91	1.93	2.22	2.00	2.73	1.97	10.84
Tatung TCS-8000 (386/20)	Aug. 88	3.04	1.74	1.18	0.94	2.41	2.98	1.13	2.09	1.92	10.53
IBM PS/2 Model 70-E61 (386/16)	Jan. 89	2.11	5.50	1.55	1.93	2.28	2.18	1.35	2.94	1.78	10.52
Compaq Deskpro 386/16	Feb. 87	2.20	1.52	1.45	1.49	2.26	2.40	1.52	2.25	1.96	10.38
Twinhead 386SX (386SX/16)	Mar. 89	1.93	4.91	1.45	1.17	2.29	2.00	1.62	2.57	1.76	10.23
Mitac 2386 (386/16)	Oct. 89	2.04	4.41	1.38	1.57	2.08	1.82	1.36	2.76	1.67	9.70
GRiDCase 1530 (386/12.5)	Aug. 89	1.76	2.69	1.55	1.24	1.78	2.01	1.81	2.17	1.82	9.58
IBM PS/2 Model 55 SX (386SX/16)	Oct. 89	1.78	4.02	1.36	2.42	2.07	1.97	1.21	2.61	1.67	9.53
GRiDCase 1535 EXP (386/12.5)	Aug. 89	1.76	2.68	1.55	1.20	1.69	2.04	1.78	2.13	1.80	9.44
Amdek System/286A (286/12.5)	Jul. 88	2.19	1.56	4.16	1.01	2.02	2.21	1.53	1.72	1.70	9.17
Dell System 200 (286/12.5)	Jul. 88	1.60	1.72	4.05	1.09	1.83	2.01	1.31	1.74	1.46	8.34
IBM PS/2 Model 50 Z (286/10)	Jan. 89	1.85	1.80	1.24	1.42	1.76	1.72	1.17	2.00	1.47	8.12
Arche Rival 286 (286/12)	Jul. 88	1.51	1.50	2.50	1.49	1.75	1.43	0.96	1.84	1.14	7.12
AST Bravo/286 (286/8)	Sep. 89	1.48	1.03	1.12	1.18	1.57	1.30	1.22	1.53	1.27	6.89
NEC PowerMate Portable (386SX/16)	Aug. 89	1.96	3.76	1.23	1.27	1.25	1.23	1.65	1.50	1.13	6.77
Leading Edge Model D2 (286/10)	Jul. 88	1.27	1.25	3.86	0.79	1.63	1.24	1.32	1.28	1.21	6.68
Epson Equity II+ (286/12)	Jul. 88	1.28	1.21	3.43	0.92	1.54	1.47	1.07	1.22	1.24	6.54
IBM PC AT (286/8)**		1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	5.00
IBM PC XT (8086/4.7)**		0.22	0.71	0.32	0.25	0.33	0.28	0.22	0.35	0.29	1.47

*System has been benchmarked but not yet covered in BYTE.
 **Listed for reference only.

BYTE BENCHMARK INDEXES—WITH MATH COPROCESSOR



BENCHMARKS AT A GLANCE

BYTE BENCHMARK INDEXES—WITHOUT MATH COPROCESSOR

Computer	Month appeared	Low-level			Applications					Cum. appl. indx.
		CPU	Disk	Video	WP	SS	DB	Sci./Eng.	Cmplr.	
Micro Express ME 386 (386/20)	Oct. 88	3.30	1.47	2.58	3.46	2.73	1.73	1.31	2.32	11.54
Gateway 386 (386/20)	Oct. 88	2.77	1.55	2.80	3.16	2.25	2.39	1.14	2.27	11.21
Fortron 386 (386/20)	Oct. 88	2.77	1.33	2.84	3.15	2.78	1.54	1.12	2.15	10.74
Zeos 386 Tower (386/16)	Oct. 88	2.61	1.97	2.25	3.08	2.67	1.54	1.05	2.30	10.64
DataWorld 386 (386/16)	Oct. 88	2.20	1.52	1.64	2.76	2.34	2.15	0.90	2.14	10.29
Spear Mono-386A (386/16)	Oct. 88	2.61	1.38	2.28	3.01	2.66	1.45	1.05	1.92	10.09
Northgate 386/16	Nov. 88	2.61	1.38	2.27	2.86	2.75	1.34	1.06	2.04	10.05
Micro 1 Power 386/20	Oct. 88	2.54	1.44	1.86	2.90	2.39	1.69	0.98	2.07	10.03
Club 386 (386/16)	Oct. 88	2.62	1.39	2.28	2.91	2.17	1.56	1.05	2.06	9.76
Whole Earth 386 (386/16)	Oct. 88	2.75	1.30	2.25	2.92	2.16	1.50	1.05	2.05	9.68
VIPC Micro 386 (386/20)	Oct. 88	2.91	1.33	1.90	2.71	2.46	1.54	1.07	1.90	9.68
CompuAdd Standard-386 (386/16)	Oct. 88	2.20	1.43	1.66	2.64	2.34	1.50	0.88	1.91	9.27
Pacesetter 386 (386/20)	Oct. 88	2.36	1.43	2.06	2.60	2.15	1.48	0.97	1.88	9.08
Suntronics-386 (386/16)	Oct. 88	2.20	1.23	2.33	2.62	2.15	1.44	0.90	1.83	8.93
Blackship 386 (386/16)	Oct. 88	2.43	1.33	1.48	2.74	2.01	1.43	0.89	1.81	8.88
Bus 386 (386/16)	Oct. 88	2.20	1.04	1.63	2.57	2.14	1.51	0.89	1.70	8.81
GCH EasyData 386 (386/16)	Oct. 88	2.42	1.34	1.84	2.45	2.00	1.50	0.90	1.90	8.75
Value 386 (386/16)	Oct. 88	2.20	1.22	1.65	2.66	2.00	1.32	0.87	1.84	8.69
PC Network THE 386 (386/16)	Oct. 88	2.20	0.93	1.63	2.54	1.97	1.43	0.91	1.83	8.67
Uniq 386 (386/16)	Oct. 88	1.87	1.26	1.50	2.47	1.91	1.45	0.82	1.78	8.44
Compaq SLT/286 (286/12)	Mar. 89	1.59	1.77	1.43	1.77	1.67	1.95	0.61	1.69	7.70
Hertz 386 (386/16)	Oct. 88	2.03	1.32	1.57	2.09	1.61	1.32	0.82	1.79	7.59
NCR PC916sx (386SX/16)	Mar. 89	1.87	1.34	1.11	2.11	1.70	1.28	0.72	1.71	7.52
Ogivar 286 Laptop (286/12.5)	Mar. 89	1.70	1.19	1.38	1.75	1.63	1.34	0.62	1.45	6.79
Zenith SupersPort 286 (286/12)	Feb. 89	1.55	1.06	1.38	1.59	1.53	1.28	0.64	1.40	6.43
Mitsubishi MP-286L (286/12)	Feb. 89	1.62	0.92	1.29	1.45	1.41	1.05	0.59	1.13	5.64
Epson Equity LT (NEC V30/10)	Oct. 88	0.93	0.61	0.82	1.01	0.86	0.92	0.34	0.81	3.94
HP Vectra CS Model 20 (V30/7.16)	Jun. 88	0.64	0.26	0.62	0.77	0.84	0.68	0.25	0.65	3.19
NEC MultiSpeed HD (V30/9.54)	Jun. 88	0.68	0.47	0.59	0.74	0.89	0.41	0.27	0.64	2.96
NEC UltraLite (V30/9.83)	Aug. 89	0.93	1.42	0.80	N/A	0.90	N/A	0.35	0.99	N/A

BYTE BENCHMARK INDEXES—MACINTOSH FAMILY

Computer	Low-level				Applications					Cum. appl. indx.
	CPU	FPU*	Disk	Video	WP	SS	DB	Sci./Eng.	Cmplr.	
Macintosh IIcx	4.61	1.15	3.65	2.58	2.72	3.25	3.07	6.13	2.79	17.97
Macintosh SE/30	4.61	1.16	3.01	2.33	2.68	3.53	2.99	5.23	2.60	17.04
Macintosh IIx	4.57	1.16	3.02	2.59	2.60	3.20	3.15	5.32	2.53	16.81
Macintosh II	3.81	1.00	2.56	2.35	2.00	2.72	2.53	4.24	2.16	13.66
Macintosh SE	1.00	N/A	1.00	1.00	1.00	1.00	1.00	1.00	1.00	5.00
Macintosh Plus	0.81	N/A	0.75	0.91	0.80	0.88	0.93	0.91	0.84	4.36

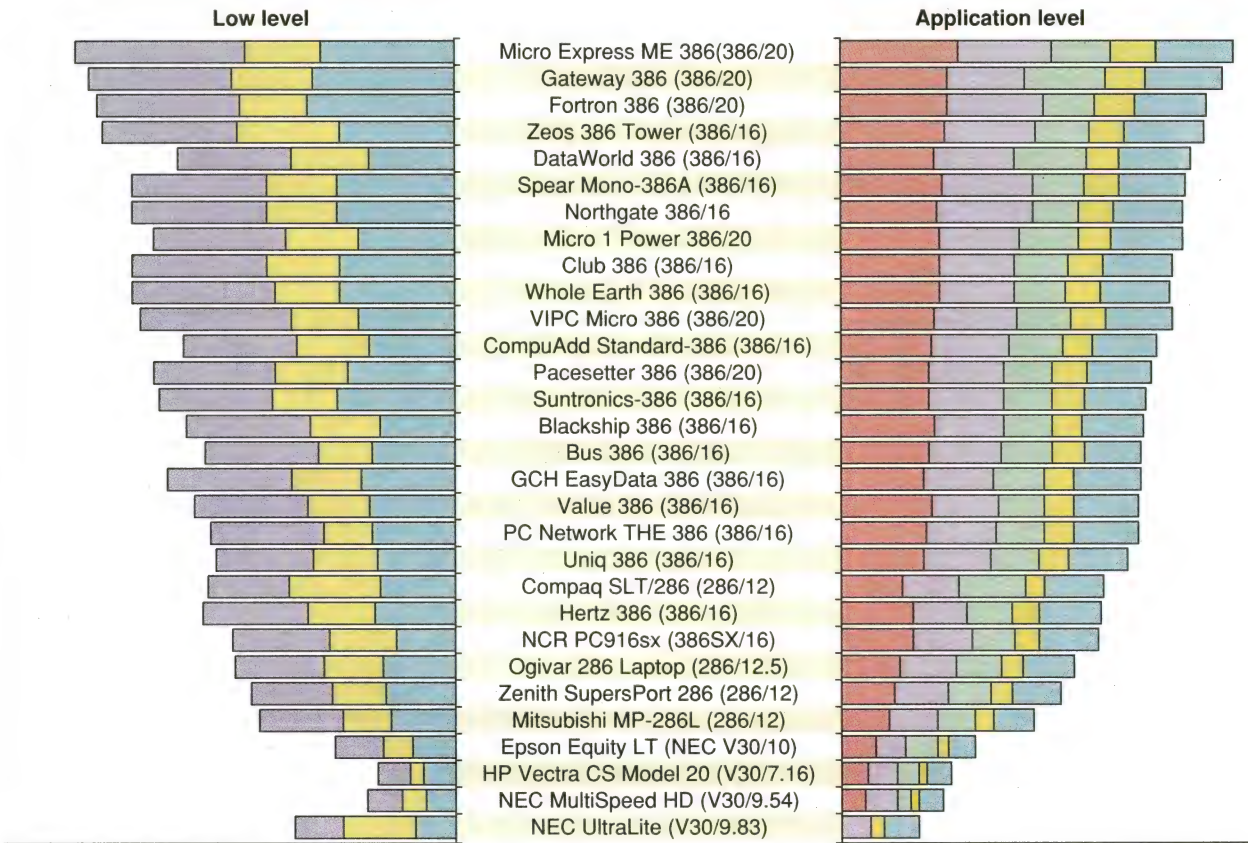
* FPU index based on Macintosh II. All other indexes based on Macintosh SE.

PC-compatible systems are referenced against an 8-MHz IBM AT with an 80287 coprocessor. The cumulative application index represents an overall score based on all application tests. The baseline AT registers at 1.0 on each application index for a cumulative index of 5.0. Therefore, a cumulative score of 20 would suggest an operating speed four times that of the standard AT. The NEC UltraLite could not run the entire set of application tests and so does not have a cumulative application index. The UltraLite's low-level bar graph is more representa-

tive of its speed since the application-level bar lacks two segments. For all graphs, the low-level bar extends to the left of the listed system and the application-level bar extends to the right.

Predictably, the 68030 machines (IIcx, SE/30, and IIx) top the Macintosh list. The 68000 processor inside the SE and the Plus does not support an integrated math coprocessor, so those machines could not generate an FPU index. For the same reason, the Macintosh FPU indexes are referenced against the Mac II, while all other indexes are based on the Mac SE. The Macin-

BYTE BENCHMARK INDEXES—WITHOUT MATH COPROCESSOR



BYTE BENCHMARK INDEXES—MACINTOSH FAMILY



CPU
 FPU
 Disk
 Video
 Word processing
 Spreadsheet
 Database
 Scientific/Engineering
 Compiler

tosh indexes should not be compared to the PC indexes.

Benchmarking can be a tricky business, especially given the wide range of methods employed to make systems run faster. For the most part, we run the systems intact, testing them the same way you would use them—as complete systems. We do disable software caching because it steals precious RAM, but hardware caching is fair game. We try to test all machines with a coprocessor installed. Machines tested without a coprocessor are listed separately. The Macintosh benchmarks have been re-

vised since the last update, so the numbers have changed slightly. The PC benchmarks have not faced a major revision since the December 1988 listing.

As systems continue to stretch the performance curve and as the 80486s start to appear, the BYTE Lab will be ready with a new generation of system benchmarks. Stay tuned. ■

Stanford Diehl is a BYTE testing editor. He can be reached on BIX as "sdiehl."



CSR 286/14



CSR 286/20 SL

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You've invested a lot in software. That's reality. So we designed our machines to be 100% compatible with all your MS-DOS[®] and OS/2[®] software.

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CSR 386/20



CSR 386/25c



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CSR 286/14 CSR 286/14 SL

- 80286 Intel based microprocessor running at 14 MHz.
- 1 MB RAM expandable to 16 MB (8 MB on the system board).*
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- High speed VGA controller.
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- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Enhanced 101 tactile "click" keyboard with copy holder and dust cover.
- Socket for Intel 80287 or Weitek math coprocessor.
- 1 parallel, 1 serial port and a Microsoft compatible bus mouse port.
- 8 industry standard expansion slots. **
- Power reset switch.
- Security keylock.
- AMI bios.
- Real time clock with battery backup.
- MS-DOS and MS-OS/2 compatible.

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80287 math coprocessor.
Slim line case with one 5.25" and two 3.5" drive bays accessible.

NOTE: *Up to 8 MB in SL case. ** 5 expansion slots in SL case.

CSR 286/14 Hard Disk Drives	Monitors / Adapters		
	Monochrome	VGA Mono	VGA Color
20 MB 40 MS ST506	\$1,699	\$2,099	\$2,399
40 MB 40 MS ST506	\$1,899	\$2,299	\$2,599
40 MB 22 MS ST506	\$1,999	\$2,399	\$2,699
90 MB 18 MS ESDI	\$2,599	\$2,899	\$3,299
150 MB 18 MS ESDI	\$3,099	\$3,299	\$3,699

CSR 286/20 SL CSR 286/20

- 80286 Intel based microprocessor running at 20 MHz.
- 1 MB RAM expandable to 16 MB (8 MB on the system board).*
- Page mode interleave memory architecture.
- High speed VGA controller.
- Track buffered high speed dual diskette/hard disk controller.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Enhanced 101 tactile "click" keyboard with copy holder and dust cover.
- Socket for Intel 80287 or Weitek math coprocessor.
- 1 parallel, 1 serial port and a Microsoft compatible bus mouse port.
- 8 industry standard expansion slots.**
- 3 speed selectable 8 MHz, 16 MHz or 20 MHz speed.
- Power reset switch.
- Security keylock.
- AMI bios.
- Real time clock with battery backup.
- MS-DOS and MS-OS/2 compatible.

Popular Options

2 MB to 16 MB of high speed memory.
20 MHz math coprocessor.
Slim line case with one 5.25" and two 3.5" drive bays accessible.

NOTE: *Up to 8 MB in SL case. ** 5 expansion slots in SL case.

CSR 286/20 Hard Disk Drives	Monitors / Adapters	
	VGA Mono	VGA Color
3.5" 1.44 MB Diskette Drive	\$1,999	\$2,299
40 MB 22 MS ST506	\$2,599	\$2,799
68 MB 22 MS	\$2,799	\$2,999
90 MB 18 MS ESDI	\$3,499	\$3,799

CSR 386/20

- Intel 80386 Microprocessor running at 20 MHz.
- 1 MB RAM expandable to 16 MB on the system board.
- Page mode interleave memory architecture.
- Socket for 20 MHz Intel or Weitek math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Track buffered high speed diskette/hard disk controller.
- Enhanced 101 tactile "click" keyboard with copy holder and dust cover.
- High speed 16 bit VGA controller.
- 1 parallel, 1 serial port and a Microsoft compatible bus mouse port.
- 200 watt power supply.
- 8 industry standard expansion slots.
- Power reset switch.
- Security keylock.
- AMI bios.
- Real time clock with battery backup.
- MS-DOS and MS-OS/2 compatible.

Popular Options

2 MB to 16 MB expansion memory options.
25 MHz Intel coprocessor chip.
Internal or external tape backup.

CSR 386/20 Hard Disk Drives	Monitors / Adapters			
	VGA Mono 1MB RAM	VGA Mono 4MB RAM	VGA Color 1MB RAM	VGA Color 4MB RAM
40 MB 22 MS ST506	\$3,099	\$4,099	\$3,399	\$4,399
68 MB 22 MS	\$3,199	\$4,199	\$3,499	\$4,499
90 MB 18 MS ESDI	\$3,699	\$4,699	\$4,099	\$5,099
150 MB 18 MS ESDI	\$4,199	\$5,199	\$4,499	\$5,499
322 MB 18 MS ESDI	\$4,799	\$5,799	\$5,099	\$6,099

CSR 386/25c

- Intel 80386 Microprocessor running at 25 MHz.
- 1 MB RAM expandable to 16 MB on the system board.
- Advanced Austek Cache memory controller with 32K of high speed static RAM Cache.
- Page mode interleave memory architecture.
- Socket for 25 MHz Intel or Weitek math coprocessor.
- 5.25" 1.2 MB or 3.5" 1.44 MB diskette drive.
- Track buffered high speed diskette/hard disk controller.
- Enhanced 101 tactile "click" keyboard with copy holder and dust cover.
- High speed 16 bit VGA controller.
- 1 parallel, 1 serial port and a Microsoft compatible bus mouse port.
- 200 watt power supply.
- 8 industry standard expansion slots.
- Power reset switch.
- Security keylock.
- Award bios.
- Real time clock with battery backup.
- MS-DOS and MS-OS/2 compatible.

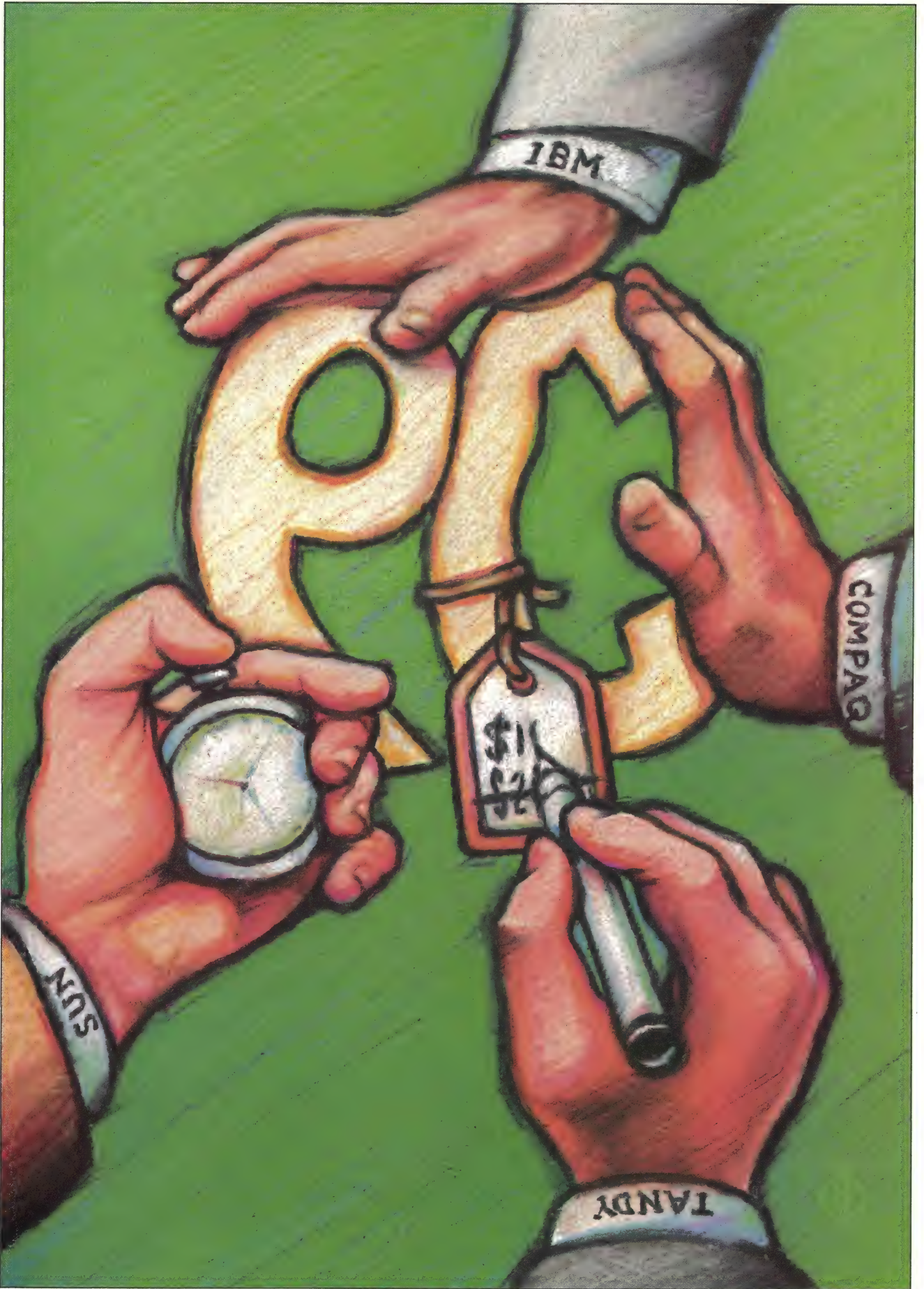
Popular Options

2 MB to 16 MB expansion memory options.
25 MHz Intel coprocessor chip.
Internal or external tape backup.

CSR 386/25c Hard Disk Drives	Monitors / Adapters			
	VGA Mono 1MB RAM	VGA Mono 4MB RAM	VGA Color 1MB RAM	VGA Color 4MB RAM
90 MB 18 MS ESDI	\$4,799	\$5,799	\$5,199	\$6,199
150 MB 18 MS ESDI	\$5,299	\$6,299	\$5,699	\$6,699
322 MB 18 MS ESDI	\$5,699	\$6,699	\$6,099	\$7,099

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REDEFINING THE STANDARDS

What did and didn't happen, what came and went, and what's coming—maybe...

Martin Heller



On the cover of the June BYTE it says "The *Fastest 386s Ever?*" Inside are reviews of real PCs running the 80386 chip at 33 MHz. That's fast—a noticeable improvement over last year's speed record, which was 20 MHz. (Between 20 MHz and 33 MHz, you briefly saw 25-MHz machines.) For software developers and others needing the horsepower—like people needing fast LAN servers—33 MHz is the new standard.

Meanwhile, Intel announced the 80486—four times faster than the 80386 at the same clock rate, with clock rates destined to go higher yet—and the 80860, a supercomputer on a chip that can also act as a coprocessor for the 80386 or 80486. When you see a real machine running an 80486 at 40 MHz with an 80860 processor, you'll be seeing a PC capable of solid modeling in real time. For engineers and designers that need such things, this scenario is a revolutionary change. Even though you can now get this sort of performance on high-end engineering workstations, having an affordable PC with these capabilities opens a whole new world.

This year, a fast PC goes at 33 MHz and performs about 8 million instructions per second. Last year, a fast PC went at 20 MHz and ran at 5 MIPS; the standards are changing quickly. Now, a "big" PC has 300 megabytes of hard disk storage, 8 megabytes of RAM, tape

backup, and a CD-ROM drive. In addition, a high-resolution PC displays 256 colors at 640 by 480 pixels, 16 colors at 800 by 600 pixels, or black and white at 1280 by 720 pixels, and it prints fonts from 6 to 60 points at 300 dots per inch. A portable PC can fit into your briefcase, with room to spare for your notepad, pens, and paperwork.

During the past few years, AT-class computers have become commodity items, and PC-class computers have become inexpensive enough to buy for home use. OS/2 caught on among programmers, but not enough OS/2 applications came out to interest users in the complexities—or RAM requirements—of a new operating system. Unix got ported to the 80386 and started looking like a possible competitor to OS/2. Lotus 1-2-3 release 3.0, dBASE IV, and a lot of other software slipped behind schedule. DOS 4.0 had so many bugs that few people upgraded from DOS 3.3.

There's a trend here—the same trend that has been characteristic of the computer industry since 1948: Computers keep getting faster, smaller, and less expensive.

Chips on silicon are getting denser and faster—but new technology is waiting to take over. For instance, RISC chips, currently used in engineering workstations, are produced both in silicon and in gallium arsenide—which can run much faster. When this technology becomes inexpensive enough for PCs, you'll see

another round of speed improvements. Further on the horizon, quantum transistors may replace bulk transistors on chips, which will lead to even more improvement.

In Search of New Standards

First, the old standards are still out there. Despite what you read, wherever the price matters more than the performance, machines using the 8088 are still alive and well. My writing's a good example: I may use a 20-MHz 80386 machine with a hard disk drive for programming, but I use a 4.77-MHz 80C88-based laptop for word processing. In other words, I don't need a Porsche when a Hyundai Excel can get me to and from the supermarket.

But there are some new standards. IBM's Micro Channel architecture (MCA) looks like it might have some uses after all. Microsoft Windows seems like it's becoming a standard for a graphical environment. At least 640K bytes of RAM per machine is a new standard, too. Others include EMS 4.0 and XMS (memory standards for expanded and extended memory under DOS), as well as the virtual-control program interface (VCPI), a standard for control programs and DOS extenders on 80386-based machines. Finally, there is OS/2, which IBM and Microsoft would like to make into the standard multitasking protected-mode operating system.

continued

Around these standards, there's a plethora of products. PCs are packaged as towers, desktops, portables, and laptops. Their processors include Intel's 8088, 80286, 80386SX, 80386, and—in the dream world of announced products not yet shipping—the 80486 and 80860.

Given identical clock rates, an 80286 is still faster than an 8088. However, the clock rate enters the performance equation, too. The original PC ran its 8088 at 4.77 MHz; turbo PCs run the 8088 as fast as 10 MHz. The original AT ran its 80286 at 6 MHz—this produced a machine that was seven times faster than a PC. Improved 80286 chips, including the CMOS 80286 variant, are powering machines at up to 20 MHz—although the garden-variety AT clone that sells for well under \$2000 probably runs at 10 or 12 MHz. Available from Intel are 80386 chips rated for speeds of up to 33 MHz; at this writing, the first few 33-MHz machines are shipping.

A 33-MHz 80386 running with zero wait states pans out at about 8 MIPS—roughly eight times faster than the DEC VAX-11/780—for ordinary integer instructions. Without a numeric coprocessor, its floating-point performance is still pathetically slow. With a 20-MHz 80387, it runs at about 220,000 floating-point operations per second; with a 20-MHz Weitek coprocessor (and software to match), it cruises at about 450,000 FLOPS.

The 33-MHz 80387, which is not shipping yet, should run at about 350,000 FLOPS. The 33-MHz Weitek Abacus has just been announced, but it should run at about 650,000 FLOPS. For CAD, CAE, and scientific computing, the floating-point performance of a computer is just as important as the integer performance—if not more so.

The announced 80486 includes the numeric processing functions of the 80387 as well as the integer processing functions of the 80386—and some additional advanced features—all on one chip. It is expected to run about four times faster than an 80386/80387 pair at the same clock rate, and Intel expects to push it to higher clock rates.

Intel has also announced the 80860, which can operate as a coprocessor to the 80486—giving even better floating-point, signal-processing, and graphics performance. Industry speculation is that the 80860 could be the basis of a desktop supercomputer. The 80860 prototype boards in PS/2s have already outperformed high-end workstations in demos. Tantalizing stuff, but a bit far off to affect this year's buying plans.

Storage, Storage, Storage

Processor performance is only part of the story in computer performance. The other part, which, in some applications (e.g., accounting), is the dominant part, is I/O performance. On PCs, there are four major flavors of floppy disks—5¼-inch and 3½-inch form factors at low and high density, giving 360K-byte, 1.2-megabyte, 720K-byte, and 1.44-megabyte capacities. All are very slow—10 times slower than the slowest hard disks. Hard disk drives can have access times as slow as 80 milliseconds or as fast as 14 ms.

Interestingly, the 720K-byte 3½-inch floppy disk was available at the time the PC was introduced. But despite its advantages, it didn't become widely accepted in the PC world until the laptop phenomenon took off late last year. Laptops (despite an FAA threat to ban them from airplanes) now seem ubiquitous.

Transfer speed is just as important as access times to a hard disk drive's performance. Four kinds of hard disk drive interface are currently available—modified frequency modulation, run-length-limited, ESDI, and SCSI. MFM, also called ST-506, is the standard; RLL is basically MFM with data compression, which buys you higher data density and faster access at the expense of reduced reliability. RLL controllers are recommended only for RLL-rated disk drives. ESDI, a technology that migrated from minicomputers to PCs, has a data transfer rate roughly twice that of MFM hard disk drives. SCSI hard disk drives don't have a fixed transfer rate—since SCSI is a systems interface and not a plain drive interface, the drive has enough intelligence to negotiate transfers with the controller. The promise of SCSI to give fast, inexpensive drives hasn't really been fulfilled yet. In head-to-head comparisons, ESDI drives still tend to outperform SCSI drives. But as SCSI drives and controllers improve, they'll probably get faster than ESDI drives.

Hard disk drives come as small as 10 megabytes and as large as 450 megabytes. It's a good bet that a 10-megabyte hard disk drive will have an 80-ms access time and an MFM interface, and a 150-megabyte or larger hard disk drive will have an access time of under 30 ms and either an ESDI or a SCSI. Whether ESDI or SCSI will dominate the high-end hard disk drive market in the future is anybody's guess. Most hard disk drive manufacturers are hedging their bets and are producing larger, faster drives with both interfaces.

For even more capacity, you have to switch from magnetic to optical disks.

There are three kinds of optical disks: CD-ROMs, WORMs (write once, read many times), and erasable optical disks. CD-ROM disks are read-only digital versions of audio compact disks. They hold 550 megabytes and are inexpensive to produce in quantity—mastering a CD-ROM costs about \$1500, and reproducing one costs about \$2 per platter. CD-ROM drives sell for about \$700.

CD-ROMs are coming of age as an information distribution medium, with about 200,000 CD-ROM drives in the field and about 600 titles—including worthwhile, readily available applications such as Microsoft Programmer's Library, the *Oxford English Dictionary*, and Grolier's Electronic Encyclopedia. However, CD-ROM drives are slow compared to hard disk drives. In addition, CD-ROM drive interfaces have not been standardized, so it is not possible to freely mix CD-ROM drives and controllers.

WORM drives are a near-ideal medium for backup and archival storage; their higher speed and low mastering costs make them a good alternative to CD-ROMs for small-audience products. WORM gear is expensive, though—drives cost about \$2500, and disks can cost \$100 each, so the economics favor CD-ROM plus a tape backup.

The revolutionary change in hard disk storage this year has been rewritable, removable optical disks—first seen on the NeXT machine and announced shortly afterward for PCs.

NeXT-style 256-megabyte rewritable magneto-optical cartridges cost \$50 for the media and \$1500 for the drive. Similar products announced for the PC list for more like \$4500. And 20-megabyte 3½-inch "floptical" disks (\$8) and drives (\$250) from Insite Peripherals also let you "carry your whole world with you." While too slow to replace hard disk drives, too expensive to use as a software distribution medium, and not likely to be widely available this year, floptical disks look like a good bet to become standard equipment on high-end PCs and workstations in the early 1990s.

For backup today, the best storage value for your money still comes on tape. High-density streaming cartridge and cassette tape drives cost about \$10 per megabyte of storage capacity—for instance, a 60-megabyte streaming cartridge tape drive goes for about \$600; the media costs about 50 cents per megabyte. And you certainly wouldn't want to back up a 150-megabyte hard disk drive onto floppy disks. Daily tape backups are

continued

Russian technology of programming TECHNOLOGY

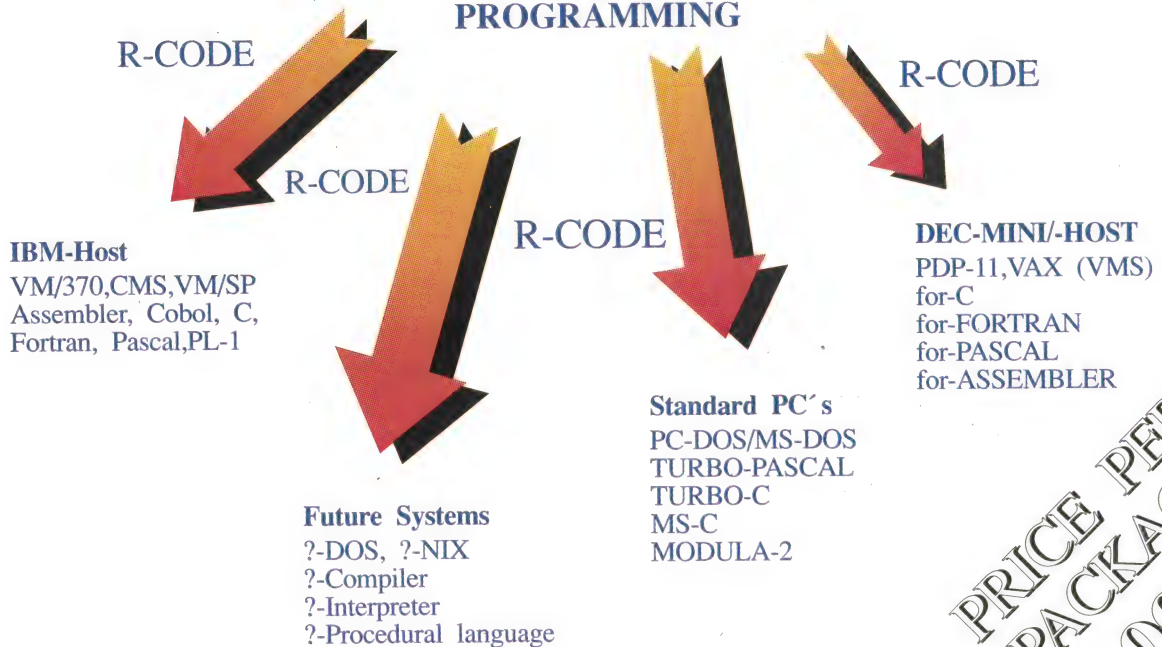


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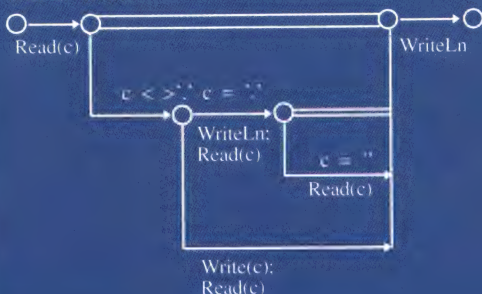
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```
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VAR c:CHAR;
```



And the same program in traditional form

```
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FROM InOut IMPORT Read,Write,WriteLn;
VAR c:CHAR;
BEGIN
  Read(c);
  WHILE c <> >'A c = '' DO
    IF c = '' THEN
      WriteLn:
      Read(c);
      WHILE c = '' Do
        Read(c)
      END;
    ELSE
      Write(c);
      Read(c)
    END;
  END;
  WriteLn:
  WriteLn;
END PrintId.
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On the cutting edge of new technology are higher-density tapes. For instance, TEAC America has a hard disk drive that stores 320 megabytes on cassettes. For even higher density, look for tape drives based on 4-millimeter digital-audio tape cassettes, which can hold gigabytes and are headed toward being able to handle terabyte capacities. Like VCRs, DAT drives use helical-scan techniques. Helical scan is a diagonal recording technique that provides for very high-density storage. Under development are cassette drives using helical-scan techniques.

Coming down the pike is *digital paper*, the latest thing in a write-once optical-storage medium. Digital paper differs from existing WORM media in that it is flexible and can be cut, stamped, and otherwise made into a variety of products, including floppy Bernoulli disks and tapes (see "Digital Paper," February BYTE). Its promise is to make smaller, faster, and less-expensive WORM drives as available for PCs as floppy disk drives are today.

Seeing Is Believing

The most obvious part of a computer is the display; today there are video options from monochrome to SuperVGA to specialized intelligent display systems for CAD/CAM, imaging, and solid modeling. SuperVGA systems can display TV-quality images; 256 colors from a palette of 256,000 gives the illusion of continuous color, and 640- by 480-pixel resolution appears photographic if given an image with continuous color.

With such a system and appropriate software, you can display a digitized or a synthesized image. Solid modeling or rendering software with Gouraud or Phong shading, such as CADKey solids, can compute and display a convincing image of a three-dimensional solid; with the addition of Pixar's RenderMan software, the solid can have natural textures, and the image can be photo-realistic. Autodesk and CADKey have both announced support for RenderMan; neither has announced when it will be available.

High-resolution color displays are good for more than displaying images; Windows, Presentation Manager (PM), and a number of other graphical user interfaces (see "A Guide to GUIs," July BYTE) virtually require high resolution. The worst-case display for Windows is CGA, whose "high" resolution turns out to be a less-than-acceptable 640 by 200 pixels in black and white. On the other hand, the right SuperVGA card with a

multiple-frequency monitor can display Windows at 800- by 600-pixel resolution with 16 colors for a combined cost of about \$1000. For about the same price, the Wyse 700 terminal displays 1280- by 760-pixel resolution in black and white.

High-resolution color images hog your hard disk drive, use lots of RAM, and stress the system. Even with the compression built into a format like GIF (for graphics interchange format), a 640- by 480- by 256-pixel color photographic image can easily take a quarter megabyte or more to store. The sheer size of such a file means it will take a while to load—anywhere from 10 seconds to several minutes. Computing such an image with even the best rendering software and PC hardware available takes the better part of an hour, and with run-of-the-mill equipment, it's an overnight job.

To deal with this problem, there are several emerging CD-ROM vision and sound standards. Digital Video Interactive (DVI) uses a highly compressed hardware/software scheme to fit an hour's worth of fully animated images and sound onto a CD-ROM, which otherwise would hold only a few minutes' worth.

For less-demanding applications, Microsoft, Philips, and Sony have collaborated on the CD-ROM extended architecture (XA), which is a variation on current CD-ROM drives that uses an adaptive compression chip and an ordinary CD-ROM drive to combine high-fidelity sound with photographic-quality images.

At the moment, CD-ROM XA demos animate an image of a few inches and synchronize it with stereo sound: "Talking heads" are within the capabilities of the technology, but the larger images that DVI produces require considerably more hardware and are still out of reach.

Back to the Bus

The original PC bus carries 8 bits of data at a time; the AT bus, also called the Industry Standard Architecture (ISA) bus, carries 16 bits. For slow peripherals, such as serial and parallel ports driving modems and printers, 8 bits of data coming from the bus is plenty. For fast disk drives, a 16-bit data path helps speed things up. However, for very high-speed devices, such as memory, even a 16-bit bus can be a bottleneck.

This problem has at least three solutions. Compaq, ALR, AST, Everex, and other manufacturers of high-performance 80386-based machines use a second, high-speed 32-bit bus for memory.

continued



PCL printers
are multiplying like gerbils. It isn't
just that they're cheaper than
PostScript printers—they're also
convenient for PCs since they print
text without any special settings.

Compaq calls this "flex architecture." The advantage of this solution is high performance, but it comes at the expense of standardization—memory-expansion boards for 80386-based systems are not interchangeable.

IBM's MCA bus supports a rich set of bus-control signals, including "bus masters." This flexibility means that MCA can support multiple processors directly. MCA also has enough grounding and shielding for a higher bus frequency—rumor has it that it can go as high as 80 MHz, or 10 times the rate of the AT bus. Unfortunately for anyone with an investment in ATs, the MCA bus is totally incompatible with ISA cards.

Extended ISA, a rival 32-bit bus standard promoted by the "Gang of Nine" (Compaq and other rivals of IBM), maintains compatibility with ISA cards. EISA members do not propose to standardize memory architectures. Instead, they intend to continue to compete in the area of memory subsystems.

Obsolete Processors?

Is the 8088 a has-been? Hardly. Even though the other Intel processors are faster, the 8088 consumes the least amount of power, especially in CMOS. This makes the 80C88 the obvious choice for battery-powered laptops. The one I use runs for 3½ hours on a little 2-amp-hour nickel-cadmium battery. And 8088-based computers are inexpensive enough (under \$1000) to be sold as home computers.

Is the 80286 without value? Not if you care how much bang for a buck you get. AT clones have become commodities—you can buy them complete with a hard disk drive for well under \$2000. If you care about multitasking, an 80386 might be a better choice, but if you are on a budget, you can do fine with an 80286.

Is the 80386SX an idea whose time will never come? Not likely. What the

80386SX chip is good for is making an inexpensive computer with the flexibility and multitasking abilities of a full 80386, but without the performance of one. Lots of applications can benefit from the 80386's memory management capabilities without requiring screaming performance—for example, desktop publishing. There's enough competition between vendors so that an 80386SX machine might not cost any more than an 80286 with the same performance.

Does anyone really need a 33-MHz 80386? Well, I do. Programming Windows and OS/2 applications exercises a computer like nothing else. Rebuilding a 300K-byte program on an XT used to take me 8 hours; now I can do it in about 15 minutes on my 80386-based ALR FlexCache with a fast ESDI disk drive.

Printers Galore

I used to have a daisy-wheel printer in my office. The output was beautiful, but when it was running I had to leave the office to preserve my hearing. So I replaced this "machine gun" with a near-letter-quality dot-matrix printer, which wasn't much better; it sounded like an air-raid siren.

A laser printer put an end to this problem. It makes less noise than a copy machine while printing immaculate text at eight pages per minute. However, at prices of about \$2000 and up, it's not for everyone. One alternative is the ink-jet printer. For about \$700, the HP DeskJet offers the same 300-dpi resolution as laser printers and the same silent operation—although at a much slower printing speed.

For desktop publishing, there's nothing like a PostScript printer. It's true that the software packages support the less-expensive Printer Control Language (PCL) printers, but these printers use up lots of disk space for holding downloadable fonts.

Up until this year, Adobe had close control of the PostScript market it created. It managed this feat by encrypting its fonts partially in the fonts themselves and partially in the PostScript controller. Adobe is so proud of its encryption that its president, John Warnock, publicly challenged anyone to break the scheme.

Hackers, however, love a challenge. Needless to say, Adobe's encryption has been broken, and it is now offering to license its technology. This opens the door for printer controllers with ersatz PostScript interpreters to use Adobe fonts, and for competing type foundries to offer PostScript fonts with Adobe encryption and *hints* (rules that improve the quality of scalable type in small sizes).

At the same time, PCL printers are multiplying like gerbils. It isn't just that they're much cheaper than PostScript printers—they're also more convenient for PCs since they print ordinary text as received without any special settings. The HP LaserJet and its descendants and imitators have sold so well that just about all software supports them.

Because of the success of the HP laser printers and because the PCL language and font formats have been openly available, numerous vendors have produced fonts for HP-compatible laser printers. In the last year, Bitstream has revolutionized the font market with FontWare. This technology can scale HP fonts to any size from 6 to 64 points.

All the high-end word processing and desktop publishing companies got into the act—Lotus started shipping FontWare with Manuscript, Microsoft included it with Word, WordPerfect included it with its eponymous best-selling word processor, and Aldus shipped it with PageMaker. At the same time, Bitstream offered a large family of FontWare typefaces for \$199 each.

Recently, several other type vendors have jumped into the fray with their own scalable font systems. Of these, perhaps the most formidable is Compugraphic. Users can only welcome the competition, which will undoubtedly bring the prices of scalable fonts down to affordable levels.

Many Tasks, Big Tasks, or Many Big Tasks?

One of the most emotional issues in the trade press this past year has been the merit of and prognosis for OS/2. The pro-IBM/pro-Microsoft camp takes the religious position that OS/2 is the ordained and logical successor to DOS. Doubters and heretics, although divided

REDEFINING THE STANDARDS

into camps favoring various alternatives to OS/2, are united in decrying OS/2 as fat, incomplete, overambitious, under-supported, and, most damning of all, associated with IBM.

At present, OS/2 is an excellent operating system that offers little or no benefit to end users. For a developer, OS/2 offers robust multitasking, transparent memory management, and excellent development and debugging tools. Given a choice between trying new code under OS/2 or under DOS, I'll always choose OS/2. Under OS/2, the bugs show up at the instruction that caused them, instead of, under DOS, resulting in a hung machine and possibly a corrupted disk directory.

For an end user, OS/2 offers only potential. Too many of the currently available applications for OS/2 are little more than ports of DOS or Windows applications. In some cases, they are better or faster or have bigger workspaces than under DOS; in other cases, something has been lost in the translation. Mostly, this situation is a matter of immaturity. OS/2 (and, in particular, PM) is still an infant system, with little user and software base.

Up until the beginning of the summer, for instance, the only PM printer driver I had was for an IBM dot-matrix printer; now I have a full set of Epson printer drivers and a PostScript driver. The generic driver with HP LaserJet support is coming—you guessed it—*real soon*.

Unix is much more mature, but it was designed by programmers for programmers. OS/2 demands at least 8 megabytes of space on your hard disk drive, and its GUI, PM, comes standard with the system. Unix demands at least 32 megabytes, and it has several competing GUIs, none of which is standard. Of these, OSF/Motif (from Open Software Foundation) has the virtue of interoperability with PM and the backing of over 100 of the players in the Unix market. But Open Look has the backing of both Unix originator AT&T and Unix International, the rival consortium to OSF.

While Unix and OS/2 both offer full-blown multitasking and virtual memory, most of the DOS-based alternatives offer only one or the other—and sometimes neither. DOS extenders, such as Rational System's DOS/16M (used by Lotus for its 1-2-3 release 3.0), offer access to all the extended memory in your machine, up to the 80286's addressable limit of 16 megabytes of RAM. This is a big improvement over DOS's 640K-byte limit, but it won't let you run a 20-megabyte program in 4 megabytes of RAM like a

virtual memory system will.

Phar Lap's 386|VMM is a full-blown, paged virtual memory system that runs a 20-megabyte program in 4 megabytes of RAM—but it is limited to pricey 80386-based systems. And neither Phar Lap's product nor Rational System's allows multitasking. A.I. Architects has a product that does both DOS extension and multitasking—but only if you buy its HummingBoard, which is essentially another computer.

DESQview allows multitasking, but it won't permit a single application to use more than 640K bytes of memory. Windows/386 allows multitasking of DOS and Windows applications, but, again, DOS applications can't have access to more than 640K bytes of memory, and the memory management used by Windows applications is somewhat limited and incurs a large overhead. To give you an idea of how much overhead, consider that when Windows 2.1 increased the memory available to Windows programs by a mere 60K bytes, PageMaker and Excel both ran three times faster.

Windows applications are, in fact, very similar to PM applications. One paradoxical result of the marketing push behind OS/2 and PM has been that Windows under DOS has flourished like never before. Microsoft is now shipping more copies of Windows than Apple is shipping Macs; somehow, I don't think that was what IBM intended.

When Is a PC Not a PC?

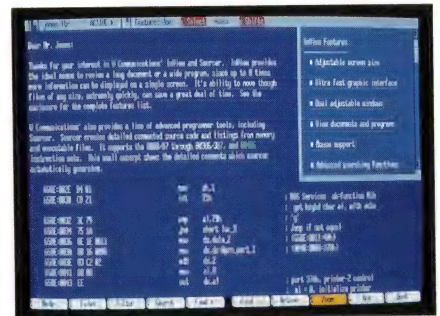
It is a tribute to the power of 20 million PCs and the applications that run on them that most workstations and minicomputers support virtual PCs. They support them in two ways: with a PC board or with PC-emulation software.

At the same time, high-end PCs are trying to be workstations and minicomputers. What's the difference between a PC and a workstation? It's not just the nameplate. Workstations come with big displays, lots of RAM and disk space, Ethernet built in, and specialized software. The very word *workstation* denotes connectivity. The phrase *personal computer* denotes isolation and autonomy.

Workstation vendors are quick to tell you that their systems and applications software make as much difference as their hardware. Workstations generally run Unix or something similar and always have a GUI; the mouse and graphics display come standard. Intense engineering applications, such as printed-circuit-board routing, take advantage of all workstation features: gobs of memory,

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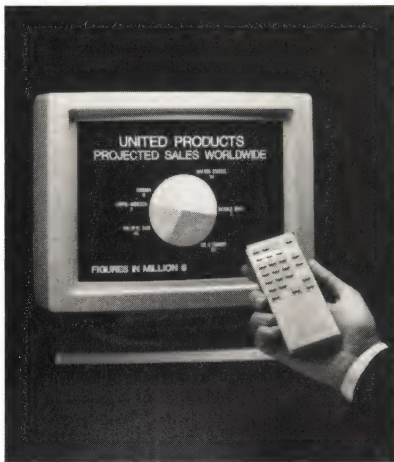
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GUIs are necessary features on a workstation for many reasons. To begin with, they look good. Don't discount visual appeal—it makes a big difference in your attitude if you're looking at something attractive. In addition, GUIs are easy to learn and easy to use. Then throw into the GUI's feature/benefit statement the advantage of interoperability among different computers and operating systems, and you have some rather compelling reasons for mice and windows. Once you have learned to use Microsoft Windows, for instance, you'll find that you already know how to use OSF/Motif and OS/2 PM.

To LAN, or Not to LAN?

PC LANs have begun to seriously challenge minicomputers as the best host for multiuser applications. You would think that computers would be cheaper by the dozen, but when you have to wire them together, the costs add up quickly.

Consider that the file server is probably a 25- or 33-MHz 80386 machine with at least 6 megabytes of RAM and 300 megabytes of hard disk space. It needs an uninterruptible power supply to avoid file and database corruption problems; its software costs anywhere from \$2000 to \$8000; and its network cards and wiring are likely to run \$500 per workstation. LANs may be cheap compared to minicomputers, but they can be pricey compared to stand-alone microcomputers, even considering the savings gained by sharing peripherals.

One way to cut the cost of a network is to use diskless workstations. MIS managers love this solution—it gives them back the control they lost when PCs started taking over from big iron. But a user on a diskless workstation is totally dependent on the availability of the file server. One little disk problem, and you have 50 people telling customers, "I'm sorry, I can't help you right now—the system's down."

Another way to reduce the cost of a network is to eliminate the file server. However, in the process, you lose some performance and features. OS/2 LAN Manager, while it embodies a client-server model, can be set up with servers running as tasks on workstations. TransM is one firm that makes a peer-to-peer network, also known as a zero-slot LAN.

There are some modems that now let PCs communicate through wall sockets. You can plug your computer in, unplug it, move it, and plug it in again; it will still be able to communicate with other

PCs equipped with this type of modem. Adaptive Networks is one of the companies that make this type of modem.

A relatively new wrinkle on the whole LAN concept is to eliminate the wires altogether. O'Neill Communications has developed a wireless LAN that uses a high-frequency radio to communicate between network nodes. The local-area wireless network is designed primarily for workgroups with as many as 20 users who want to share peripherals, such as laser printers or modems, to transfer files, and to send and receive E-mail. A LAWN doesn't allow file sharing, and its operating system won't support client/server applications.

Although the \$495 cost per node of a LAWN is higher than most low-end or zero-slot LANs, which run as low as \$100 per node, O'Neill Communications claims that the savings from not having to wire up a network more than compensates for the difference.

The Yellow Brick Road

What's happening in IBM's Oz? If you look down the yellow brick road, you'll see faster, smaller, and less-expensive PCs. You'll also see standardized window-icon-mouse-pixel interfaces across all computing platforms and operating systems, and transparent data exchange among different brands of computers, whether they run DOS, OS/2, Unix, VMS, or Pick. Along with optical-storage facilities, helical-scan tape backup devices will become popular.

But if the past is any guide, you're in for some surprises. What will be the next new application area for PCs—next year's equivalent of desktop publishing or distributed databases?

The most striking thing about PCs this year, though, isn't how fast they run or how portable they are or how much graphics resolution comes in how many zillion colors or how they network; it's something much more subtle. PCs have done more than join the mainstream of computing; by their very numbers and practical importance, they have *become* the mainstream of computing. PCs aren't "toys" beneath the contempt of MIS and corporate computing managers anymore. PCs are an essential, ubiquitous part of the computing toolkit in businesses large and small, in academia, in science and engineering, and in publishing. ■

Martin Heller develops software and writes about technical computer applications. He holds a Ph.D. in physics. He can be reached on BIX as "mheller."

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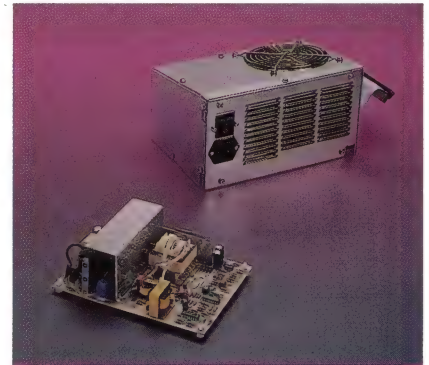
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THE 80486: A HARDWARE PERSPECTIVE

By putting the math coprocessor and cache controller on-chip, Intel shows that the whole can be greater than the sum of its parts

Ron Sartore

By now, you probably know that Intel's 80486 consists of a "souped-up" 80386 processor, an enhanced 80387 coprocessor, an integral cache controller, and 8K bytes of static RAM (SRAM) all rolled into a 1.2-million-transistor package. You've probably read and reread all the marketing explanations and rationale behind the 80486 (see the text box "The Economics of Performance" on page 68). But have you thought about the *real* aspects of constructing a well-behaved, high-performance AT system around the 80486?

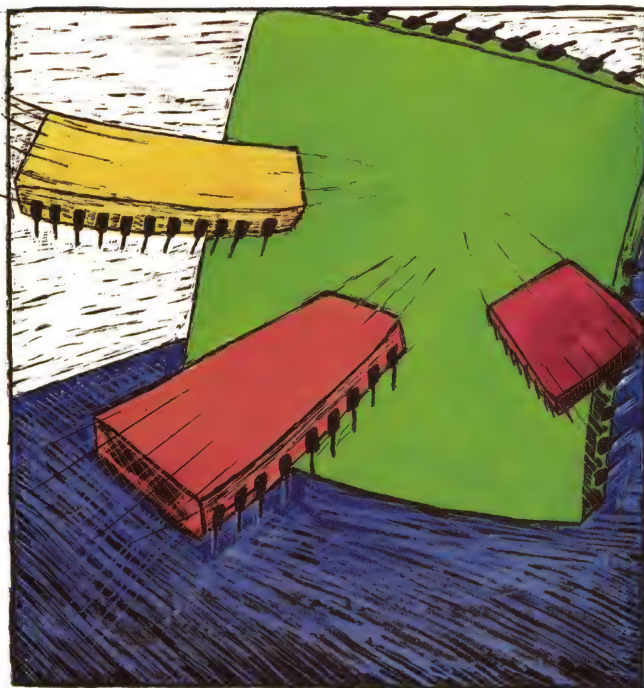
On the Pins

A comparison of the 80386 and 80486 pin-outs reveals 36 more pins on the 80486. Some extra pins provide more power connections to the device, some allow the proper use of the newly integrated caching and coprocessor elements, and others can be considered outright new features. Many have been left as "no-connects"—pins that you can truly leave unconnected—that will be available to future software development tools or to provide a method for specific manufacturing circuit

testing or programmability. Because Intel has not publicly defined the 16 no-connect pins, system designers and designers of printed circuit board layouts can immediately say: "Our project is already 10 percent done." Unfortunately, completion of the job comes with more difficulty.

Table 1 shows the pin-out differences between the 132-pin 80386 and the 168-

pin 80486. The designers eliminated four of the 80386's pins, added 20 pins to allow for integrated and new features, and threw in 19 inert logic pins. All the remaining 129 pins can be considered logically identical. I guess that makes the project 88 percent complete now ($129 + 19 / 168 = .88$). Piece of cake. The text box "The New Pins on the Block" on page 70 provides a short description for each new signal.



What's New?

It may be instructive to think of the 80486's new features as three different kinds of "hooks": cost-reduction/convenience hooks, performance-improvement hooks, and future hooks. Some of the new features hit combinations of these. The easiest new signal to categorize is the pin that identifies transfers to an 8-bit device (the /BS8 pin). This pin is an obvious cost-reduction/convenience feature because it enables the 80486 to recognize and adjust itself to devices that can accept only 8-bit transfers.

On the other hand, the signals involving bus ownership and control (there are three of these) in conjunction with the six pins used to manage the

continued

The Economics of Performance

Gene Sumrall

If the laws of supply and demand continue to function as they have in the past, you may be able to purchase an 80486 system for less than some comparably configured 33-MHz 80386 systems. When you total the cost of a 33-MHz 80386 CPU, a 33-MHz 80387 math coprocessor, and a 33-MHz 82385 cache controller chip, you come up with \$991. That's \$41 more than the cost of the 25-MHz 80486 chip. The comparison becomes even more lopsided when you consider that the 33-MHz 80386 design requires expensive static RAM and glue logic that raises the ante even more. It becomes laughable when you consider the difference in performance.

It's interesting that Intel should initially price the 80486 chip lower than a not-so-comparable 33-MHz 80386 chip set. Intel certainly knows that the 80486 is considerably faster and has more features, and that PC manufacturers will gladly pay a premium for it. From a cost point of view, 80486 systems should sell for less than 80386 systems. From a performance and functionality point of view, 80486 systems should sell for much more. Intel has provided the best of both worlds: relatively low cost and high performance. Eventually, supply and demand will correct this odd situation, presumably by reducing the market price of the 80386 chip sets.

What's the Cost?

You may reasonably ask, "If the cost of the 80486 chip is less, will an 80486

system cost less?" Based on Intel's initial pricing of the 25-MHz 80486 and the 33-MHz 80386 chip sets, it appears that the answer is yes. There is, however, a small problem.

The first 80486 chips will be in short supply. If Intel distributes them in the same way that it did the 80386 chips, initial shipments will go exclusively to the major PC companies and large distributors of PC components. If history repeats itself, the first 80486 systems may list for more than \$15,000. As the volume of 80486s increases, shipments will find their way to the smaller, more competitive PC companies, and that's when you should see an interesting phenomenon.

Assembling a hypothetical \$15,000 80486 system, dollar by dollar, should prove instructive. The CPU will cost \$950, a price set by Intel. An 80486 system board, less CPU and memory, should have a street value of about \$2750. Add in \$800 for 4 megabytes of memory, and you still have \$10,500 left to spend. A case, a 250-watt power supply, and a quality keyboard will cost another \$400. Then you include the standard 1.2-megabyte floppy disk drive, and, while you're at it, add a 1.44-megabyte floppy disk drive just to be safe. With a 100-megabyte ESDI hard disk drive and a 1-to-1 interleave controller, this adds about \$1400.

You now have \$8700 left. A quality 14-inch VGA multisync monitor and VGA adapter card should be no more

than \$650. And now the hard part: You must find an adapter board with two serial ports and one parallel port for less than \$8050. If you can find one for about \$45, you have succeeded in building a base model 80486 for \$6995. This is less than some comparably configured 33-MHz 80386s.

Family Planning

When Intel introduced the 80486, it made a promise to the PC world that went something like this: "If you develop operating systems and software for the 80386 instruction set, you can depend on having a solid platform for the next 10 years and beyond." Every major hardware and software company in the industry has given the Intel 80386 instruction set its blessing. Predicting the future of the PC industry has never been easier—it will be based on the 32-bit 80386 instruction set. The least common denominator has been defined.

Predicting the obvious is easy; converting that knowledge into a purchasing strategy for the 1990s is the hard part. Perhaps I can help here. You can immediately eliminate any processor that does not have the ability to run the 80386 instruction set. Then your choice is between three members of the Intel family of 80386-based chips.

The baby of the family is the 16-MHz 80386SX, previously known as the P9. Think of the 80386SX as a fast 80286 chip that has the ability to run 32-bit 80386 code at a miserably slow pace. If

80486's cache appear to contain all the essential ingredients to construct multiple 80486 machines. The implicit software development needed to take full advantage of such a hardware-concurrent architecture is realistically five to 10 years in the future. (If that sounds pessimistic, look at how far protected-mode code for the 80286 and 80386 has gone!) See the text box "The BIOS Challenge" on page 72 for more details on utilizing the 80486.

The "new-feature" pins that provide for a significant (though subtle) performance advantage—ignoring the cache and coprocessor—are the ones associated with the parity path and the address bit 20 gating. I'll go into the details of how the parity path and address A20 gate in-

crease the system's performance later in the article.

A History of Memory Demands

Back in 1985, when the first volume shipments of zero-wait-state memory add-ons for the AT became available, users would ask: "What's a wait state?" Today, performance is recognized to be gauged almost solely on the number of wait states between the processor and the memory subsystem. Yet the wait-state question is still as valid (and more complex) today as it was then.

In 1985 the processor of distinction was the 80286 (and then only at 6 and 8 MHz). The 80286, with its coarse clock granularity, made zero-wait-state operation relatively straightforward (i.e., an 8-

MHz 80286 would require a memory access to be complete within 125-nanosecond clock increments—125 ns, 250 ns, and 375 ns correspond to zero, one, and two wait states, respectively).

Late in 1986, 80386 processor systems emerged with 16-MHz clock speeds. Now wait states were measured in increments of 62.5 ns, and systems were unable to achieve true zero-wait-state performance using conventional DRAMs. Many (somewhat unethical) suppliers, attempting to boost their 80386 specifications, claimed (wrongly) that they were running zero wait states when in fact they were running with one or two. Actually, they were using the 8-MHz 80286 as the yardstick. Their fear was that if they advertised their machines as

you are absolutely certain that you will continue to run primarily DOS, with a few OS/2 applications mixed in, the 80386SX could be a possible choice. Like the other members of the 80386 family, the 80386SX has the ability to simulate EMS 4.0 in extended memory. No special expanded-memory boards are required; software does the trick. If you use programs such as DESQview or Lotus 1-2-3, this could be justification for purchasing the 80386SX as opposed to a fast 80286 system. But when you consider that a true 32-bit 80386 system costs only a few dollars more, the 80386SX is not your best choice.

The true 32-bit 80386 (the DX series) is available in four flavors: 16-MHz, 20-MHz, 25-MHz, and 33-MHz. Systems based on the 16-MHz and 20-MHz versions of the 80386 series are obvious winners in the low-end 80386 marketplace. They offer exceptional value as compared to the 80386SX at about the same price. It is reasonable to expect that, in time, the prices of 25-MHz and 33-MHz chips will drop and that they will take the place of the slower chips.

It's a given that the 80486 will dominate the high end of the PC market because it has no competitors. If you are thinking of buying a 25-MHz or 33-MHz 80386, you should now seriously consider the 80486 as an option.

Gene Sumrall is cofounder of Cheetah International, Inc., in Longview, Texas. He can be reached on BIX c/o "editors."

executing at anything *but* zero wait states, the machines would have been perceived as running slower than a no-wait-state 8-MHz AT clone.

As Intel improved clock speeds on the 80386, the memory speed demands exceeded the capabilities of conventional DRAM architectures. Following the history of mainframes, main-storage SRAM caches became common in high-speed 80386 systems. These high-speed SRAM caches were able to achieve zero-wait-state operation *most* of the time. Many benchmarks ran as never before, yet not all applications reflected the improvement indicated by the benchmark. Why? Well, ignoring applications that were truly I/O bound, certain applications kept thrashing the cache, and the

job of keeping the contents of the fast SRAM valid fell right back on good old DRAM.

From table 2 (which represents an optimistic, high-performance implementation), it is apparent that many so-called zero-wait-state systems are reading a different spec sheet than Intel's. Table 3 shows a similar comparison for both the 25- and 33-MHz 80486.

The Burst and the Pipeline

The major memory-access difference between the 80386 and 80486 (excluding the 80486's on-chip cache) is pipelined versus burst operation. The 80386 has a feature called "pipelined access" that was not fully utilized by most systems or entirely effective in some situations. Pipelined access presented the address of the next access—if available and at the system's request—so that memory could have a head start on that next access. A good concept, yet it appears that it was often utilized only to keep the 80386's instruction prefetch buffer full. (The instruction prefetch buffer assumed that a series of linear sequential addresses would be the next required code and tried to maintain four words resident within the chip.) Often this effort proved to be nothing more than memory busywork, thus creating the undesired side effect of keeping the DRAM system in a nonoptimal situation for fast access. Pipelined memory writes were also hampered by not having the data until after a pending read was completed. (The pipelined write could not proceed until the data from a preceding pipelined read left the data bus.) The perfect hurry-up-and-wait scenario.

Armed with 20/20 hindsight, Intel saw that the intended function of the 80386's instruction prefetch buffer was nothing more than a poor man's cache. Put the cache on-chip, chuck the prefetch mechanism as we know it, and—voilà— instant 80486. As to the pipeline mechanism, it's a good concept (maybe pipelined bursts are to come on the 80586), yet in the 80386 implementation it still took two clock cycles per transfer, whereas the 80486 burst mode takes only one. To state it simply, the 80486 burst-transfer mechanism represents a twofold increase in data transfer rates over the equivalent 80386 clocked approach.

Burst mode, an old mainframe bus technique, rightfully assumes that most of the delay in accessing main storage is in the connection time to retrieve a specific data address. Once the initial access occurs, adjacent or neighboring data is readily available without the formal pro-

Table 1: Pin changes for the 80486. The total of added pins yields 39—four pins more than expected—until the defunct 80386 pins are removed.

New feature pins

Parity path	5 pins
Burst transfers	2 pins
AT A20 emulation	1 pin
8-bit bus interface	1 pin
Bus ownership and control	3 pins

New "forced-feature" pins

Cache controller	6 pins
Coprocessor	2 pins

New inert pins

Ground	7 pins
Power	4 pins
No-connects	8 pins

Dropped 80386 pins

No pipelining	1 pin
Coprocessor/ CPU interconnect	3 pins

cedure required of the first access. You may recognize the burst concept under a different name: nibble mode, video RAM, page mode, or any block transfer mechanism. Even disk drives have endorsed this technique, albeit under the name "multiple sector transfers." Memory bandwidth is greatly enhanced by this concept.

A quick calculation of the system's memory speed requirements to support the 80486 burst mode reveals an amazingly obvious memory architecture. Given that the chip has one clock to transfer data to and from memory and that the preferred memory device would be DRAM, how can you utilize the relatively slow and less expensive DRAM? Remember, the 80486 already has an on-chip SRAM cache.

The answer lies in the fact that a key element of bandwidth is *width*. Even for the 33-MHz 80486, true zero-wait-state burst cycles can be achieved by using DRAM. This is possible by structuring the 80486 main memory as 64 bits wide. The initial access to the memory requires only one true wait state, while the subsequent accesses are already present. The third and fourth accesses of the burst each then utilize the clocked page-mode mechanism to achieve zero wait states. The implementation of this approach is not difficult or unwieldy, and a 60-ns DRAM array organized in a 64-bit-wide architecture is capable of achieving a

continued

The New Pins on the Block

Here's a list of the 80486 processor's new pins. They are categorized by function, with descriptions of what they'll mean for upcoming systems built around the 80486.

Parity Path

DP0-DP3: The four parity data path (I/O) pins allow less external logic and faster memory interface than on the 80386.

/PCHCK: The *parity checker* output pin signals a parity error and emulates the AT memory parity-check function. Note that the system must decide whether to pay attention to this error. For example, RAM on video boards carries no parity component and so will likely generate a parity error that the system can ignore.

Burst Transfers

/BRDY: The *burst-ready* input pin indicates that the current cycle is complete and that the system will assume data transfer in the next clock cycle unless signal **/BLAST** is presented.

/BLAST: The *burst last* output signifies that burst-transfer mode is done.

AT A20 Emulation

/A20M: This input is the address bit 20 mask. When the system asserts **/A20M**, address bit A20 from the CPU is forced low (under 1 megabyte). This function was previously implemented by the AT to maintain 8086 compatibility.

8-bit Bus Interface

/BS8: The system board provides the *bus size 8 bits* input signal in response to a transfer request when the desired system element can execute only 8-bit transfers. On 80286 and 80386 proces-

sors this function was handled through external hardware.

Bus Ownership and Control

BREQ: The *bus request* output signal indicates that the CPU needs the address/data bus. BREQ lightens the task of designing well-behaved multiple-processor systems.

/BOFF: With the *back off* input, an external system device (another processor, perhaps) can take control of the entire address/data bus, even within an active, yet incomplete, cycle.

/PLOCK: Intel defines the *pseudolock output* signal as a bus cycle definition. From a system viewpoint, it appears to be more of a pseudo-bus-priority bit. When the processor asserts this signal, it's saying "Don't take the bus away now; I've transferred only part of the data I wanted." This differs from the **/LOCK** bit, which typically signifies a critical *read-modify-write* operation in which no other system element can examine the item being modified until the current operation is complete.

Cache Control

/KEN: The system is required to control the *cache enable* input through hardware. In practice, rather than being used to enable cache, this signal is most frequently used to disable areas of memory that cannot be cached. System implementations vary, but for most AT machines, the area of memory between 640K bytes and 1 megabyte should *not* be cached because it holds I/O-controlled and externally swapped data. Caching it proves futile or disastrous.

AHOLD, /EADS: The *address hold* and *external address strobe* inputs allow an

external device to present the 80486 with an address. If that address matches an address in the 80486's cache, the associated data is flagged as invalid. For an AT single-processor machine, only direct-memory-access cycles would require use of this mechanism. In a multiple-processor implementation, this invalidation would likely occur from another processor.

/FLUSH: The *flush cache* input could be considered the "punt" approach to cache management. Essentially, it informs the 80486 that the entire contents of its cache are invalid. Why would you need this? Consider one 80486 electronically switching between two completely different memory systems. Each time the processor switched to a new system, its entire cache would be invalidated. With proper management of the other signals (i.e., **/KEN**, **/EADS**, and **AHOLD**) this should be a last resort.

PWT, PCD: The *page write-through* and *page cache-disable* output pins reflect bit settings in internal registers. While **/KEN** allows hardware to control the caching of specific physical regions of memory, these pins indicate caching control that software has exerted over logical memory pages.

Coprocessor

/FERR: The *floating-point error* output pin is similar to the 80387's error pin and is used under certain conditions to generate interrupt 13 on ATs.

/IGNNE: The *ignore numeric processor error* input pin has no effect if not properly activated by software. I assume that this pin will be properly managed by an unannounced coprocessor. For now, this an elaborate no-connect.

sustained processor/memory transfer rate of over 88 megabytes per second in burst mode.

Here's how it works on the 80486 using DRAM (organized for a 64-bit-wide data bus):

Clock cycle 1: The CPU initiates access.

Clock cycle 2: The memory is not ready; add a wait state.

Clock cycle 3: Transfer the first

word; assert burst ready to the 80486. Start 64-bit access of the next page.

Clock cycle 4: Transfer latched contents of memory (the second word); assert burst ready.

Clock cycle 5: Transfer the third word (paged); assert burst ready.

Clock cycle 6: Transfer the fourth word (paged); assert burst ready.

Here's how it would play on the 80386

(best case with zero-wait-state cache and assuming a cache hit):

Clock cycle 1: CPU initiates access.

Clock cycle 2: Memory responds with the first word.

Clock cycle 3: CPU initiates access.

Clock cycle 4: Memory responds with the second word.

Clock cycle 5: CPU initiates access.

Clock cycle 6: Memory responds

continued



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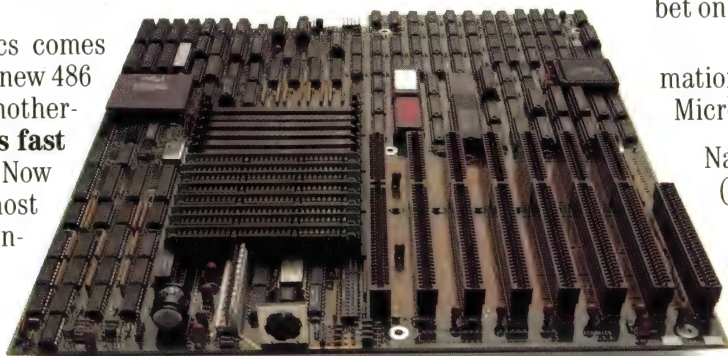
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The BIOS Challenge

René Vishney

The 80486 processor has taken AT architecture to a new plateau. Throughout Award Software's development of a BIOS for the Intel 80486 (in conjunction with Cheetah International), our benchmark tests have shown performance to be significantly greater than existing 80386 processor architectures with a cache controller and math coprocessor. Benchmark tests will need to be rewritten to reflect this performance improvement.

An 80386 BIOS will run on current implementations of the 80486, but without the 80486 BIOS you won't experience the improved performance of the built-in cache controller and math coprocessor. Using an 80386-style BIOS on an 80486 would be like using an 80286 BIOS on an 80386 machine. The critical hardware and relatively minor software differences between the 80386 and 80486 technologies are the keys to understanding how the 80486 BIOS can give users the full benefit of this new technology.

Not the Same

Intel has incorporated many new features into the 80486 that allow it to support multiple processor systems. Other significant enhancements include an on-board math coprocessor and an on-board cache controller. These additions will help remove the processor-speed bottlenecks that are characteristic of current 80386 systems. The associated increased performance of the 80486 has proved to be greater than the obvious combination of an 80386, an 80385 cache controller, and an 80387 math coprocessor system. To put it tritely, the whole is greater than the sum of its parts.

Power-on self-test operations have also been improved in the 80486. The 80486's loop timing allows the entire POST routine to run faster than on an 80386. Now that the cache is on the processor, the BIOS includes a POST cache-memory test. The POST math coprocessor routine is also faster now that the coprocessor is no longer outside of the CPU. Award's POST routines flash the chip's version number on the chip on the screen, making life easier for field technicians and system developers.

Timing Is Everything

Since the last IBM PC AT 8-MHz update, 80286/80386 processor speeds have doubled and tripled. Using timing loops that depend on processor speed has been invalid for several years. You've got to use other methods within the AT architecture to find a reliable real-time base. Two such methods are available on the 80486. The first utilizes a refresh timer that can reliably return 30-microsecond time bases. Award's 80486 BIOS uses this method for the timing of "slow" devices such as floppy disk drives and hard disk drives.

The second method involves timing between accesses of external chips to the processor, such as the direct-memory-access controller and the interrupt controller (i.e., the CPU has to wait a few clock cycles for a peripheral chip to become ready). Timings of this sort require delays of several microseconds. The only time base available is through executing CPU instructions that consume a known number of cycles. Cache controllers for the 80386 have caused some problems in this area as guaranteed times for instruction fetches have been reduced. There are several nondestructive instructions that you can use to "spin the wheels." By experimenting, we found that we could use more or less the same delay instructions on the 80486 that we used on the 80386, even at the greater speeds.

Minor Software Differences

In terms of software, even at the BIOS and operating-system level, there are few differences between an 80386 and an 80486. These differences will require changes at the system level but should not affect upward migrations of 80386 applications to the 80486.

The software differences involve the on-chip math coprocessor and the cache controller. Some flags used to interact with the math coprocessor in protected mode behave differently. Intel has also added new instructions to control the initialization of the internal cache. The only functional effects on the BIOS are differences in initialization. For example, a previously nonfatal error in coprocessor initialization becomes a fatal processor error.

Protected-mode operating systems or applications will need to change methods for trapping coprocessor instructions. Such changes will be well worth the effort; initial benchmarks have shown an order of magnitude of improvement in the performance of floating-point instructions. Most packages on the market now are conservative in their use of floating-point instructions, even in applications that double in performance with a coprocessor. Most standard systems do not contain a coprocessor for cost reasons. Developers simply cannot afford to write applications for only 10 percent of the potential market. The bulk of the compiled code still uses floating-point emulation.

For example, C's `floor()` function, commonly used in comparisons, can use floating-point libraries. This type of code would normally compile with emulation; a true coprocessor would be restricted to more time-critical areas. However, because the 80486 guarantees the availability of a floating-point coprocessor, applications can be packaged with all sections of the code utilizing floating-point, which will provide greater overall performance.

Intel is encouraging a joint effort to develop a standard method for software applications (primarily operating systems) to identify the processor type and revision of the 80486. The intent is to begin planning for future extensions to the processor family. If these efforts become a standard, they will also be applicable to the 80386 architectures already in the field with the appropriate BIOS changes. In fact, the 80486 will require BIOS products to evolve to provide a stable platform for software in this market.

Wide Open

The 80486 processor will open up many new possibilities in hardware design.

The work on fully utilizing the 80486 through the BIOS has only begun. BIOS products for it will constantly be updated, upgraded, and introduced as new capabilities become available throughout the 1990s.

René Vishney is president of Award Software, Inc., in Los Gatos, California. He can be reached on BIX c/o "editors."

with the third word.

Clock cycle 7: CPU initiates access.

Clock cycle 8: Memory responds with the fourth word.

You should realize that the above comparison shows the 80386 in its very best light. Also, the 80486 has an on-chip cache that frequently relegates the main memory to the chore of efficiently filling the on-chip cache—a chore well-performed by the burst-transfer mechanism of the 80486.

The use of a 64-bit-wide DRAM architecture does present some challenges to a system's minimum memory configuration. For example, implementing this approach with 1 megabit \times 1 DRAMs would require 72 devices, yielding a total of 8 megabytes minimum of system memory. Each expansion to this approach would also be in 8-megabyte increments. Using 256K \times 4 DRAMs solves the memory granularity problem for this 64-bit architecture but complicates the parity data path by requiring the inefficient use of 1 megabit \times 1 DRAMs or the mixing of current-technology (256K-bit \times 4) with older-technology (256K-bit \times 1) DRAMs (i.e., you would need one 256K-bit \times 1 DRAM—parity—for each pair of 256K-bit \times 4 DRAMs). Furthermore, many currently available high-density single in-line memory modules (SIMMs) do not provide for the mixing of DRAM technologies. These obstacles are not actually technical problems, but they do present a real conflict in attaining minimum system costs while achieving highest system performance.

Problems Solved

Writing parity-checked data to main memory on 80386 systems has always been trouble, because the fastest you could generate the parity checkbit was 17 ns after you were presented with valid data from the CPU. This wreaked havoc with control logic because it alone represents half a wait state for a 33-MHz system. Should you complicate the control of the parity data bit during writes by treating it separately? Or should you penalize read access time to accommodate the write constraint?

Happily, Intel's engineers plugged this hole on the 80486 by adding a parity path. Now when all data bits are valid on the data bus, that includes the parity bits. Thank you, Intel.

The 80386 still bears the scars of the 8086's migration upward through the 80286. One particularly visible injury was Intel's handling of address bit A20.

Table 2: *The 80386 zero-wait-state comparison (nonpipelined read). All times are in nanoseconds. All CPU timings are from the Intel 1989 Microprocessor and Peripheral Handbook, vol. 1 (Intel Corp., 1989).*

CPU speed	16 MHz	20 MHz	25 MHz	33 MHz
Zero-wait-state access budget	125	100	80	60
Address valid delay (from CPU)	-36	-30	-21	-5
Address buffers (CPU to memory)	-6.5	-6.5	-6.5	-6.5
Data buffers	-4.5	-4.5	-4.5	-4.5
Data setup to CPU	-11	-11	-7	-5
Remaining time for zero-wait-state memory device	67	45	40	29
Remaining time for one-wait-state memory device	129.5	95	80	59
Remaining time for two-wait-state memory device	192	145	120	89

Table 3: *The 80486 zero-wait-state comparison (nonburst-mode read). All times are in nanoseconds.*

CPU speed	25 MHz	33 MHz
Zero-wait-state access budget	80	60
Address valid delay (from CPU)	-22	-19
Address buffers (CPU to memory)	-6.5	-6.5
Data buffers	-4.5	-4.5
Data setup to CPU	-5	-5
Remaining time for zero-wait-state memory device	44	35
Remaining time for one-wait-state memory device	84	65
Remaining time for two-wait-state memory device	124	95

In the 8086 world, no address could go beyond 1 megabyte (there was no address line A20). Computed addresses beyond the 1-megabyte limit would "wrap back" into low-order memory. IBM's AT designers rightfully maintained that compatibility through the 80286. They accomplished this by masking off (jamming inactive) the address A20 line through a control spigot from the keyboard controller chip.

Brilliant, right? Not quite. Remember the zero-wait-state calculations in table 2? Well, those figures don't compensate for a slow address line A20. So hardware designers were expected to insert a logic

level (an additional delay) within the system to perform this task. The result is that when an address is asserted on the address bus, every line *except* A20 becomes valid in a specified time. Thus, for the memory speed requirement to achieve the zero wait states shown in table 2, you must *subtract* a good 7 ns. That's a 10 percent slowdown to a 70-ns memory.

Fortunately, Intel engineers came to the 80486's rescue again. They've added a line into the chip that, when active, tells the chip to operate its A20 line to emulate the action of the AT's A20 line.

continued

No major logic here, but a major performance boost. It's obvious that the semiconductor group at Intel had an excellent system mouthpiece (their board group? IBM? other users?) to champion this cause. Bravo!

What They Missed

The 80486 contains so many great system features that to criticize any part of it seems almost blasphemous. My personal gripes with the chip are relatively minor at 25 MHz but become substantial when you extrapolate operation at 40 and 60 MHz. I base these opinions not on RISC versus CISC issues, but on the more fundamental issues of the physics of electronics.

System implementers have had their hands full "managing" a common I/O bus at 33 MHz. The difficulty lies in avoiding *bus contention*. Data travels along the bus from a source to a destination (memory to CPU or vice versa), and bus contention occurs when—in the process of switching from one source to another—two sources are present on the bus simultaneously. To the layman, I can best describe this as a brief short circuit.

As
processor clock speeds
increase, the physical
properties of electronics
remain the same.

To the engineer, this presents reliability and manufacturing problems if not given proper attention.

The problem is exacerbated as system-memory speeds increase. Given the electronics components currently available to system designers, the quickest they can turn off or "shut up" a bus source from driving a common bus is about 11 ns. This suggests that, in theory, ultimate usable processor speed is limited to 45 MHz. And even as processor clock speeds continue to increase, the basic physical properties of electronics aren't going to change. As useful as common

data I/O bus 80486 is (if you consider multiple 80486 systems), it is not a desirable architecture in a 60-MHz single-processor implementation.

The solution? Separate the data lines on the CPU into DATA OUT and DATA IN. (Hey, at \$1000 a chip, what do a few more pins cost?)

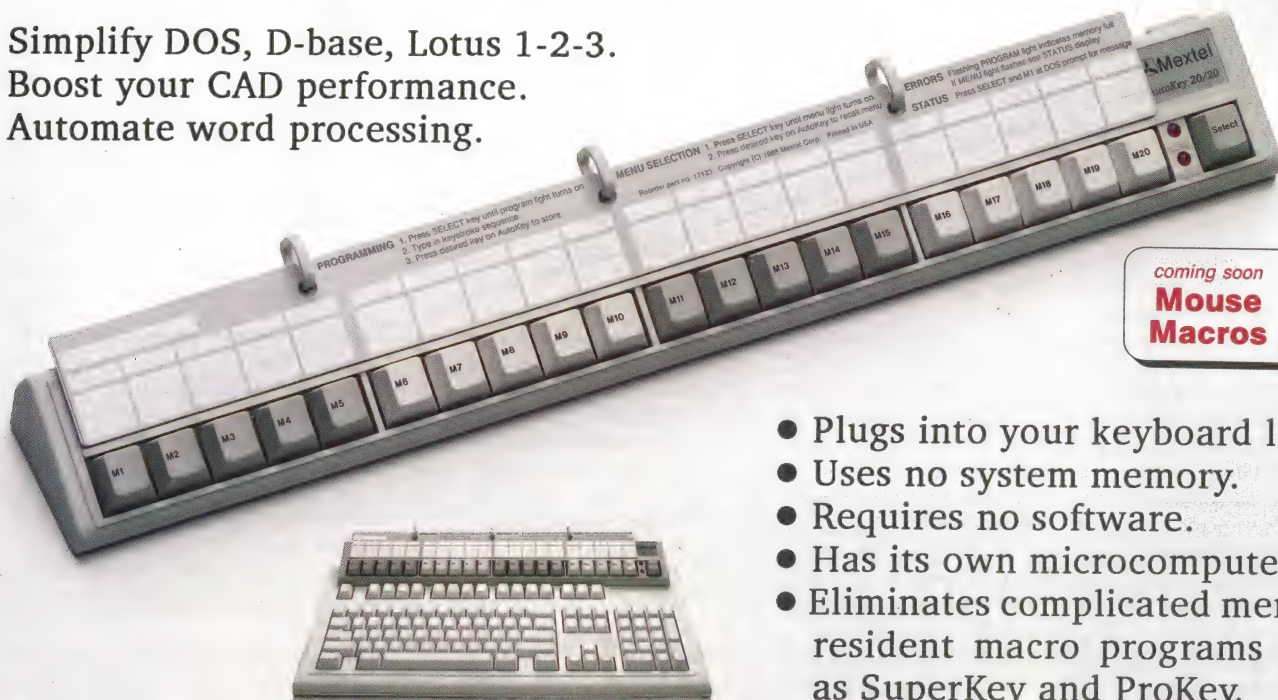
The 80486 represents a logical growth of the PC-compatible standard. That says a lot. The large base of applications software that has been established for the 80x86 is unparalleled in computing's short history. The 80486 promises to be a major commitment by Intel to software development maturation and stability. The job of hardware is to provide the reliable vehicle to maintain and enhance this desirable goal.

All CPU timings for the 80386 come from Intel's 1989 *Microprocessor and Peripheral Handbook*, vol. 1. All CPU timings for the 80486 are from Intel's manual, 80486 Microprocessor, April 1989 (#240440-001). ■

Ron Sartore is cofounder of Cheetah International, Inc., in Longview, Texas. He can be reached on BIX c/o "editors."

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The Era of the Personal Workstation

When in 1981 the first personal computer from IBM was introduced to the market, no expert predicted its success. After only one year, this computer set a new standard, the PC standard. Of course, there were other computers, like the Apple II. Some of these computers were faster and more reliable than the IBM PC. But the standard was set by this machine. And it was set by the users, who bought this computer and demanded applications, programs, peripherals and services. A whole industry grew up with this one machine. The personal computers of today are the great-grandchildren of this little computer. One can find its roots in nearly every personal computer that works with MS-DOS. When the IBM PC was introduced, it worked with MS-DOS, too. It was MS-DOS 1.1, the first release. And it became standard as an operating system, just like the PC became standard as THE personal computer.

The technology today is far more advanced than it used to be in 1981. This an effect of the tremendous market power, which was unleashed by the PC standard. But know, the great history of this standard has become a burden, it slows down any development in this industry, which is bound to be "compatible". Today's microprocessors have more processing power than the big mainframe computers in 1981. But they use only 5-10 percent of their real abilities for the users, because of the existing industry standards. We at Bauer Systems think it's time for a new standard, it's time for the PERSONAL WORKSTATION!

Stop! This is not a break with the reported history of computers. It's a break with compromises, which were made to have the highest grade of compatibility. We have found a way to have the best of both sides: Unforeseen processing power and user friendliness and compatibility with existing industry standards. We cannot promise that your most beloved word processor will run on our new machine, and we cannot promise either that your beloved screen will work with our machine. But we can promise you that if you ever try our new system, you will not try another existing computer again.

The TESS IV PERSONAL WORKSTATION is based on the Intel i486 microprocessor. This microprocessor combines the features of the 80386 microprocessor and the 80387 arithmetic coprocessor together with a sophisticated cache management unit on one chip. The i486 microprocessor has a raw processing power of 14-15 MIPS. In the TESS IV PERSONAL WORKSTATION, this microprocessor is combined with 8 Megabyte of 70 ns dynamic random access memory. The system has a clock rate of 25 MHz. Early benchmarks indicated a processing power of 12 MIPS for the whole system. We developed a configuration for this system, which represents the best combination of available options. The TESS IV PERSONAL WORKSTATION is equipped with our i486-computer. We chose a SCSI host adapter as storage interface. In the standard configuration, one 200 megabyte hard disk drive and one 3.5" Floptical disk drive are connected to the host adapter. It offers a sustained data transfer rate of 1 megabyte per second and it can handle up to seven SCSI devices. The hard disk drive has an access time of 16 ms. The Floptical disk drive is a newly developed 3.5" floppy disk drive that is able to store up to 20.8 megabyte of data on a 3.5" Floptical diskette. It can also format, write and read standard 3.5" diskettes in the PS/2 formats. The Floptical disk drive has an access time of 65 ms. The graphics subsystem of our TESS IV PERSONAL WORKSTATION contains its own Texas Instruments TI 34010 graphics processor, clocked at 40 MHz. At this clock rate, the TMS 34010 has a processing power of 6 MIPS. The processor is combined with 1 megabyte VRAM for a maximum screen resolution of 1024 x 768 pixels in 256 out of 262,144 colors. Our display features a 21" flat-type screen offering the user an optimal viewing area. The etched, non-glare 0.31 mm dot pitch CRT allows for brilliant FULLSCREEN graphics and text. A built-in dynamic focus circuit provides crisp images on-screen. The keyboard of our TESS IV PERSONAL WORKSTATION is connected to the screen and contains a standard 102 keys AT-layout. A 3-key mouse is connected to the keyboard as the standard pointing device.

The TESS IV PERSONAL WORKSTATION is equipped with four serial and two parallel external interfaces. It can be expanded by plug-in expansion cards compatible to the ISA-bus interface. The complete system except the desktop devices is mounted in a trim desk-side tower case in a unique design. It is powered by a 300 W switching power supply with build-in battery backup and surge protection.

To unleash the full processing power of the i486 microprocessor, we chose the newly developed Open Desktop from SCO as operating system. Open Desktop features the full 32-bit, multiuser, multitasking capabilities of the UNIX System, a graphical user interface offering Presentation Manager-compatible "look and feel", the industry-standard X Window System, SQL database management, TCP/IP networking to dissimilar systems, full data sharing between DOS and UNIX Systems, and instant access to thousands of existing DOS and UNIX System applications. Open Desktop delivers the multitasking computing power, friendly graphical interface, and seamless connectivity required for today's demanding business and technical professionals who require dedicated personal productivity systems. And it's equally well-suited as a multiuser, multitasking platform for workgroups of 8, 16, 32 or even more users.

To meet the high standards we set ourselves by designing this computer, we developed a sophisticated distribution and service system. The TESS IV PERSONAL WORKSTATION will be distributed by the microtronics Trade Service through field consultants. Your computer will be set up at your site and configured to your demands. The microtronics Trade Service will provide worldwide on-site service for one year. If your system can't be repaired on-site, you will receive a equal replacement for the repair time.

To receive more information or to purchase your TESS IV PERSONAL WORKSTATION, please contact the microtronics Trade Service. We hope you will be with us in the era of the personal workstation!

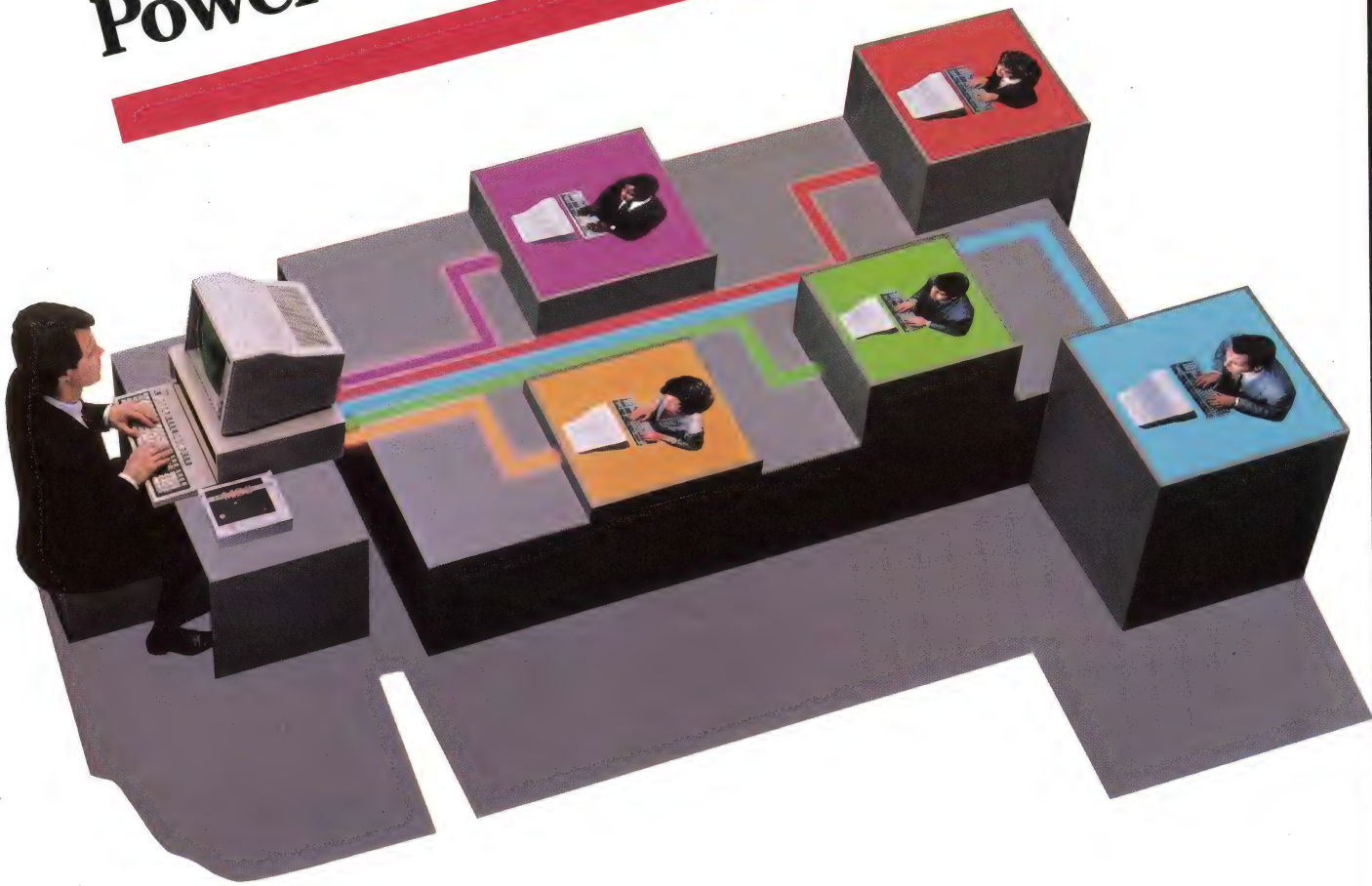
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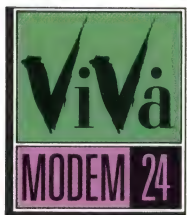
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STRETCHING DOS TO THE LIMIT

VCPI brings order to DOS multitaskers, DOS extenders, and EMS emulators

Frank Hayes

Two years ago, OS/2 sounded like a dream come true. No more applications that had to squeeze into 640K bytes; no more overlays; no more cobbling together collections of TSR programs and utilities to create a useful work environment. With OS/2 running on an 80386-based PC, programs could be as large as necessary—and you would be able to run as many as you needed, concurrently.

But OS/2 hasn't yet delivered on its promises. Two years later, we're still waiting for OS/2 for the 80386, and we're still waiting for applications software that will turn the current 80286-based OS/2 from a great idea into a great operating system. Once that software does arrive—and it should be checking in over the next six months or so—OS/2 will become a contender.

But if OS/2 hasn't already generated the applications it needs to become a best-seller, it has intensified demand for its features: big programs and multitasking. Software publishers have responded by offering multitasking systems, DOS extenders, and EMS emulators that enable DOS programs to tap the full power—

and full memory—of 80386-based PCs. Until now, though, these have largely been independent, ad hoc solutions; for example, there has been no guarantee that a program using a DOS extender would run under a multitasker.

Enter VCPI

In late 1987, six companies—including Phar Lap (386|DOS-Extender), Quar-

terdeck (DESQview), and Qualitas (386Max)—set out to agree on a standard that, they hoped, would create some order out of the burgeoning chaos of ad hoc solutions. The result, several drafts later, is the Virtual Control Program Interface, or VCPI.

VCPI isn't a program. In fact, it isn't even the outline for a program. It's just the specification for how a VCPI-compatible program should behave. But it isn't vaporware, either: Lotus has joined the original members of the VCPI committee, and all the members are busy making their software conform to the VCPI specifications. And applications developers using VCPI DOS extenders and multitaskers are also aiming for VCPI compatibility.

VCPI is designed to solve two main problems that show up when several 80386-aware programs run at the same time: conflicts over the use of extended memory, and conflicts over which one of several programs is in charge.

The original six sponsors of the VCPI were A.I. Architects, Phar Lap Software, Quadram, Qualitas, Quarterdeck Office Systems, and Rational Systems. The original

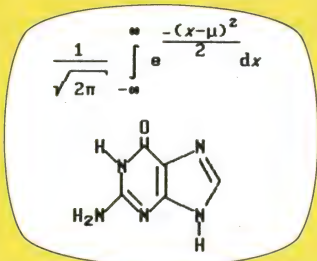
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PC Magazine, July 1988

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STRETCHING DOS TO THE LIMIT

specification was developed by Phar Lap and Quarterdeck and was published in December 1987. A more detailed and explicit revision of the spec was drafted in March of this year for the April VCPI Developer's Conference. At that conference, Lotus Development added its name to the list of sponsors, and Compaq and Intel were among the observers. The specification went through two more revisions before the final version was approved in June.

The complete VCPI specification is available from Phar Lap Software, Inc., 60 Aberdeen Ave., Cambridge, MA 02138, (617) 661-1510.

Who's the Boss?

Unlike real multitasking operating systems, such as Unix or OS/2, DOS is designed for one user running one application program. As a result, from its earliest days, a DOS program was traditionally written with the assumption that it was the only car on the road. That was fine when it was true. But as soon as users began adding pop-up TSR utilities, each application program found itself sharing memory with other programs. If the programs didn't all follow the rules (or at least cheat in regular, predictable ways) conflicts were sure to arise.

The same problem, only magnified, appears when a multitasker tries to squeeze several full-scale application programs into memory at the same time. That's cheating the limits of DOS, and if all the programs don't cheat predictably, they'll step on each other's toes.

Fortunately, the 80386 CPU features two modes—protected and virtual 8086—that can alleviate some of these problems. In protected mode, software has full access to all the capabilities of the 80386, including all its most powerful instructions and the entire 4 gigabytes of memory that can potentially be stuffed into an 80386-based PC. Once the CPU is in protected mode, it can switch into virtual 8086 (or V86) mode. When software runs in V86 mode, the CPU and memory act as if they're running on an 8086 with its own 1-megabyte (or less) cohort of memory—hence the name "virtual 8086."

But although a program runs in V86 mode as if it's in a single chunk of memory, it may actually be split up all over the 80386's available memory in smaller, 4096-byte pieces. Moreover, although the CPU appears to act like an ordinary 8086, there are some instructions that can't be used in V86 mode. When the CPU encounters one of those instructions, it generates an exception, which

returns the processor to protected mode.

Protected and V86 modes greatly simplify multitasking on an 80386. Each ordinary DOS application can run in V86 mode as if it had its own CPU and memory; the multitasker itself, which switches among the different applications, runs in protected mode, handling exceptions and generally directing traffic.

If all the programs running under a multitasker are ordinary DOS applications, this arrangement works fine—the multitasker is the unquestioned boss, running in protected mode. But multitaskers aren't the only programs that use the 80386's protected mode. Programs built with DOS extenders use it, too.

A DOS extender creates a run-time environment that lets a program run under DOS but still use the more powerful capabilities of the 80386. Since DOS doesn't run in protected mode (where the real power lies), a DOS-extended program starts out running in V86 mode. But when it's time to kick into high gear, the V86 program calls the DOS extender, which jumps into protected mode to access large amounts of memory or to execute specialized instructions.

There's also a third category of programs that use protected and V86 modes: EMS emulators. An EMS driver lets a DOS program swap blocks of memory into and out of the memory-address space above the DOS 640K-byte limit but still below the 1-megabyte limit of the 8086 CPU. The original EMS memory boards worked with any PC or XT; several extra megabytes of memory could be swapped in and out, so a program could get fast access to lots of extra space for data or program overlays. An EMS emulator uses the same set of protocols, but, instead of using memory on a separate board, it uses the 80386's own memory above the 1-megabyte limit. Once again, the DOS program runs in V86 mode; when it calls the EMS driver, the CPU kicks into protected mode so the driver can access the extra memory.

Each of these kinds of "control programs"—multitaskers, DOS extenders, and EMS emulators—needs to switch back and forth between protected and V86 modes. However, the 80386 is designed so that only one protected-mode program will handle the exceptions generated by V86-mode applications. That means that if you try to use them all together—say, an EMS emulator with a multitasker that's running one or more DOS-extended programs—only one control program can use protected mode; the others must use V86 mode. But, as I've

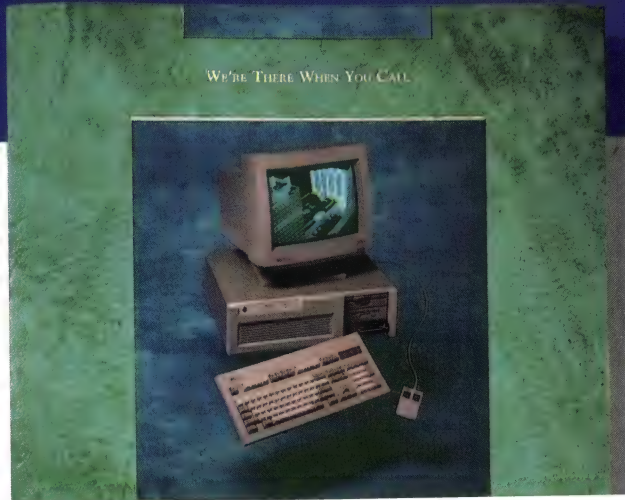
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Extended-Memory Allocation Techniques

The three techniques that VCPI allows for allocating extended memory—the memory above the 1-megabyte address boundary—are EMS allocation, top-down allocation, and bottom-up allocation. Using EMS memory is the easiest of the three; it involves nothing more than requesting pages of memory through the standard EMS 4.0 interface. Using EMS memory has another advantage for DOS-based applications; even if an application isn't running on an 80286- or 80386-based PC, it can still use EMS memory if an EMS memory card is installed.

Both top-down and bottom-up allocations depend first on knowing how much extended memory is available. That information is available from the BIOS extended-memory-size system call (Int 15h, function 88 hexadecimal). This function returns the amount of extended memory in K bytes. It's a simple matter to convert that number into the highest address occupied by extended memory: You shift the value left 10 times to multiply by 1024 and then add 100000h (1 megabyte). If function 88h of Int 15h returns 0, that means there's no extended memory in the system.

Top-down memory allocation is straightforward; it only requires lowering the memory ceiling, as indicated by the result of the extended-memory-size call. To do this, a program installs a new interrupt handler for Int 15h, one that passes all functions except 88h and returns a new, lower value for that function. Thus, in a multitasking situation, any other program that wants to allocate extended memory from the top down will first make its own call to Int 15h function 88h—and carve off its chunk of memory beginning where the first program's chunk left off.

Bottom-up allocation, by contrast, uses the technique that was originally used in IBM's VDISK driver for the AT. VDISK allocated memory for a RAM disk by installing a new interrupt handler for the PC reboot interrupt, Int 19h. A signature block and an allocation-size marker go in the interrupt handler, and a boot block with an allocation-size marker goes at the 1-megabyte boundary. Whether or not the bottom of extended memory has been carved off by VDISK or a similar program, it's possible to raise the floor still further by installing another interrupt handler

and a new set of signature blocks and allocation-size markers.

If this sounds more complicated than top-down allocation, it is. Unfortunately, the process has to be more complex than it should be. It's necessary to check both the boot block and the interrupt handler for the size of the memory that's already been allocated, since some functions (such as the DOS 3.3 PRINT function) will wipe out some of the allocation information in one of the two locations. Still, it's possible to do; from the Int 19h vector, you can trace a 24-bit value that points to the first free byte of extended memory, and you can get the same value from the boot block at offset 1Eh, which is the address in K bytes; shifting it left 10 times gives the actual address.

By installing interrupt handlers and allocation-size markers, each program in memory can allocate as much available extended memory as it needs without interfering with other programs' allocations. However, once memory has been allocated, it cannot safely be deallocated and the original interrupt handlers restored until all programs are finished using extended memory.

shown, they all need to be in protected mode—or, at least, they need a way to let each control program use protected mode. That's where VCPI comes in.

Sharing Extended Memory

A second problem that can show up once an EMS emulator and several DOS extenders have been stuffed into memory together is that they may all want to use parts of extended memory (i.e., memory above the 1-megabyte boundary).

There are four basic ways for a program to make use of extended memory. One is to simply use it, no questions asked—but that almost guarantees problems when more than one program is in memory at once.

Two other standard techniques treat extended memory as a big chunk of memory from which a piece can be carved off either the top or the bottom end: *top-down* and *bottom-up* extended memory allocation, respectively. Both of these techniques require the programmer to install a new interrupt handler for an operating-system function. In the case of top-down allocation, which lowers the

extended-memory ceiling, it's the BIOS extended-memory-size system call (Int 15h, function 88 hexadecimal). In the case of bottom-up allocation, which raises the extended-memory floor, it's the PC reboot interrupt (Int 19h). Because all programs in memory share these interrupts, each one can, in turn, carve a chunk off the top or the bottom of extended memory without interfering with the other programs. (See the text box "Extended-Memory Allocation Techniques" above.)

There's one other common technique for allocating extended memory—an EMS emulator, which uses top-down allocation to acquire a block of extended memory and then parcels out sections of it through the standard EMS interface. Since there's only one EMS emulator in memory, it's also shared by all the programs that want to use it; thus, programs won't unintentionally interfere with each other if they get their memory through the EMS emulator.

VCPI allows programs to use extended memory through top-down or bottom-up allocation, or through the EMS emula-

tor. The EMS emulator typically plays the most crucial role, because it handles VCPI functions.

How VCPI Does It

Table 1 lists the VCPI functions that an application program can call while it's running in V86 mode. Each function is called through the EMS interrupt (Int 67h), using a function call that's illegal for an ordinary (non-VCPI) EMS emulator. The VCPI function calls allow each application to switch to protected mode and determine EMS and extended memory availability (as well as get access to certain 80386 registers and interrupt controller information). Table 2 lists the VCPI functions available to applications once they are in protected mode.

How does it typically work? When DOS boots up, it installs an EMS driver whose name is in the CONFIG.SYS file. That EMS emulator—called the "VCPI server"—will handle all VCPI functions. A user can then run a DOS-extended application—or a multitasker, which in turn will run regular or DOS-

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Table 1: *The V86-mode interface is provided through the EMS interrupt (Int 67h), with a function code of DEh in the AH register and a VCPI function code in register AL. The function calls allow an application to switch to protected mode, determine availability of and allocate EMS and extended memory, and get access to 80386 debug registers and interrupt controller information.*

THE VCPI VIRTUAL 8086-MODE INTERFACE

Subfunction	Purpose
00h: VCPI Presence Detection	Checks for the presence of VCPI.
01h: Get Protected Mode Interface	Sets up the client's page table.
02h: Get Maximum Physical Memory Address	Initializes client's memory management data structures.
03h: Get Number of Free 4K Pages	Returns the total number of 4K-byte pages available to be allocated out of the server's EMS memory pool.
04h: Allocate a 4K Page	Allocates a 4K-byte page of memory.
05h: Free a 4K Page	Frees a page of memory previously allocated with subfunction 04h.
06h: Get Physical Address of 4K Page in First Megabyte	Returns the physical address of a 4K-byte page in the first megabyte of the V86-mode linear address space.
07h: Read CR0	Returns the current value of the CR0 register.
08h: Read Debug Registers	Stores the values of the debug registers into an array in memory.
09h: Load Debug Registers	Loads the debug registers with the values in the array.
0Ah: Get 8259A Interrupt Vector Mappings	Returns the interrupt vectors that will be generated by the 8259A interrupt controller when a hardware interrupt occurs.
0Bh: Set 8259A Interrupt Vector Mappings	Used by the client to inform the server if it remaps the 8259A interrupt controllers.
0Ch: Switch from V86 Mode to Protected Mode	Switches CPU to protected mode, sets up all system tables for the client, and transfers control to the specified entry point in the client.

Table 2: *The protected-mode interface is a FAR entry point in the EMS emulator. The address of the entry point is obtained during initialization with the Get Protected Mode Interface system call (Int 67h, function DEh, VCPI function 01h). An application running in protected mode makes a FAR call to a USE32 segment, with an EMS function code of DEh in register AH and a VCPI function code in register AL.*

THE VCPI PROTECTED-MODE INTERFACE

Subfunction	Purpose
03h: Get Number of Free 4K Pages	Returns the total number of 4K-byte pages available to be allocated out of the server's EMS memory pool.
04h: Allocate a 4K Page	Allocates a 4K-byte page of memory.
05h: Free a 4K Page	Frees a page of memory previously allocated with subfunction 04h.
0Ch: Switch from Protected Mode to V86 Mode	Switches CPU from protected mode back to V86 mode after setting up all the server's system tables.

extended applications.

Each application can make use of EMS memory and VCPI functions once it knows for sure that they're available. That requires a series of checks: First, the program checks to see if the CPU is an 80386; if so, the program looks for an EMS emulator; if it's there, the program turns the EMS emulator on by allocating one EMS page, putting the CPU into V86 mode; finally, the program uses VCPI function 0 to test whether VCPI is available through the EMS driver.

From that point on, the application can deal with extended memory and jump into protected mode through VCPI calls while still enjoying the advantages of running under DOS. (Of course, if the EMS driver doesn't support VCPI, the program will have to make its own arrangements for protected mode and extended-memory support.)

Of course, VCPI does require a certain amount of extra work on the part of each control program. For example, each control program must maintain its own set of system tables, which it shares with the VCPI server. Also, the control programs—and applications—must always use VCPI to switch into protected mode and then back to V86 mode.

What Hath Not OS/2 Wrought?

Is VCPI a replacement for OS/2? Not really. VCPI isn't a multitasking operating system with all the trimmings—it's really just a kludge that reduces a bit of the anarchy that was bound to arise when single-tasking, 640K-byte-bound DOS came face-to-face with a demand for multitasking and big applications. From that point of view, VCPI is just an attempt to stretch DOS's life out a little longer.

But if it's a kludge, it's a critically needed one. And right now, VCPI has two big advantages over OS/2. First, multitaskers and DOS extenders that use the VCPI are available today. They run DOS applications that are tried and tested, and they're the same familiar DOS programs that have been used for years—without the likelihood of new bugs or changes that could creep in during a rewrite to run under OS/2.

Just as important, you need at least 4 megabytes of RAM to do anything substantial under OS/2. VCPI doesn't require that much memory. In that respect, VCPI may be the perfect answer for users who already have an 80386-based PC and need to tap more of its power—but can't afford the cost of OS/2. ■

Frank Hayes is a BYTE news editor. He can be reached on BIX as "frankhayes."

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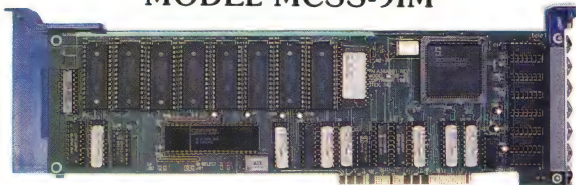
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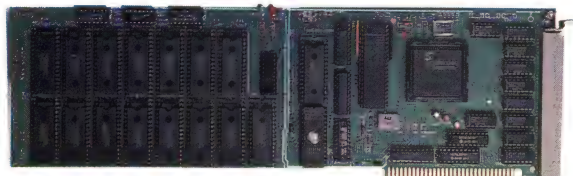
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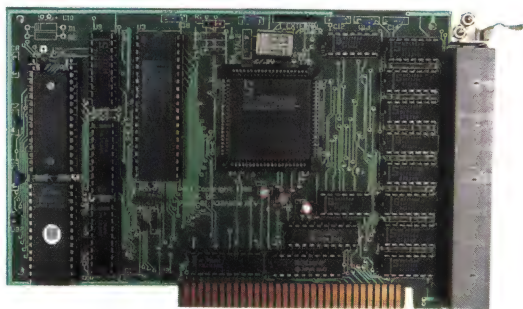
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THE STATE OF OS/2

OS/2, longer in ascendancy than planned, has a very bright future

Mark J. Minasi

Well, it's clear by now that OS/2 is a flop. It just never made the grade. Only a few hundred software vendors are writing programs for it, and only 400 programs are currently available.

Huh?

Yes, we all read that "OS/2's not going to make it" stuff in the trade press. But, then, the trade press needs *something* to write about. OS/2 is actually not doing badly, all things considered. First, I'll give a little historical perspective, and then I'll look at what's out there for OS/2 now. What can developers do in building OS/2 applications that they couldn't do under DOS, and are they doing those things? Also, I'll look at a few examples of unique OS/2 applications.

Looking Back at DOS

Examining the history of DOS in the same way that OS/2 has been scrutinized would lead you to conclude that DOS is a real flop. As of early June, 400 OS/2 applications were shipping—not DOS programs that can run in the DOS-mode session, but protected-mode OS/2 programs. By the time you read

this, 100 more programs should be available.

Here's a look at DOS's record. The following examples are from two computer magazines: an IBM PC-specific trade publication that published a comprehensive list of available software for the PC in September 1982 (one year after the PC's release) and BYTE's first IBM PC special issue in the fall of 1983.

The 1982 *IBM PC Product Guide* sports full-page ads from the big vendors. Corvus, of course, was the only company offering hard disk drives for the PC. Ashton-Tate was offering to "make your micro work like a mainframe" with dBASE II. A lot of game programs. Some snappy ads for a new kind of program, called Context MBA, that incorporated spreadsheet, database, and graphics all under one roof. Lotus 1-2-3 wasn't to appear for a year yet. Excluding games, 600 programs were available for the IBM PC one year after its release. Of the 600, nearly a third were for program development—compilers, utilities, and libraries.

BYTE's first special issue on the IBM PC was actually a regular issue (November 1983) that featured several articles about the PC. By this time, the PC had been around for slightly over two years. The debate about whether or not it would endure had dissolved. However, the market still had some growing to do. My copy has a dog-eared page so I could easily find an ad for an interesting new compiler called Turbo Pascal.

Jerry Pournelle wasn't even using a PC yet, although he

continued



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BYTE May 1989

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mentioned in his column that he would be getting one soon. One author in the issue claimed that the PC would be popular because (1) Digital Research's CP/M-86 would catch on with the release of its DOS emulator and (2) Logitech would soon release a Modula-2 compiler for the PC that would open the door for loads of new applications to be written.

Back to the Present

Today, OS/2 looks similar to DOS in 1982. Getting started costs about the same amount of money. Back then, a 256K-byte PC with two floppy disk drives (essential for development), a dot-matrix printer, an editor, and a compiler cost about \$4500. Starting OS/2 with an 80286-based machine, an 80-megabyte hard disk drive, EGA, 4 megabytes of RAM, and basic software tools runs about \$5000.

A sizable proportion of the software available now for OS/2, although not the majority, is useful mainly to developers. And the learning curve is steep. The terminology of graphical programming interfaces, threads, queues, dynamic link libraries, and the rest takes some getting used to. But in 1981, who knew what "segments" and "offsets" were, or how to (or why to) hook BIOS vectors. The sole documentation on assembly language code was the IBM/Microsoft Macro Assembler manual, which explained nothing except which op codes were which. The MASM manual had no examples of actual assembler programs and no tutorial information.

The OS/2 development situation is, in some ways, better than the DOS situation was at the one-year mark. Developers understand the iapx86 architecture, although some relearning is needed to work with protected mode. And OS/2 documentation and third-party references are more plentiful than DOS books were in 1982. OS/2 is still a bit unstable, but compare it to DOS 1.0. Early DOS wouldn't support serial printers and most utilities (e.g., BASICA and DISK-COPY). Also, it wouldn't use the full 640K bytes, and hard disk drives weren't supported. Vendors had to patch COMMAND.COM to make devices work!

Current OS/2 Applications

One source of application information for OS/2 is IBM and Microsoft's *Operating System/2 Application Guide*. (To get a free copy, call (800) 426-2468, ext. 120.) The guide lists these 13 application categories (with the number of applications in parentheses): accounting (160), business (140), communications (100),

database (82), desktop publishing (17), engineering/scientific (78), graphics (66), industry-specific (240), miscellaneous (27), spreadsheet (5), tools (142), utilities (70), and word processing (14).

Note the profusion of industry-specific products—vertical-market packages. This mimics the DOS experience.

The accounting category contains, well, accounting packages. Business is a potpourri of everything from device drivers for WORM (write once, read many times) drives to more accounting packages.

Two companies, GammaLink and Pacific Image, are offering fax boards and software—an ideal offering. Fax boards and PCs together have the advantages that they eliminate the need for a separate fax machine, print in higher resolution, and print on laser paper rather than the slimy fax paper. But they are less than perfect because they can't provide a 24-hour-a-day incoming fax service unless you're willing to dedicate a PC to faxing—which makes PC-based fax pretty expensive—or unless you run the fax board in a multitasking operating system. OS/2 and fax, then, are made for each other. A package from Inset Systems, HiJaak, will convert fax image formats to and from other graphics standards (e.g., .PCX, .DRW, TIFF, and .PIC) and just about any file format you can name.

Communications includes the usual array of 3270 and VT-100 emulators, as well as X.25 and TCP/IP gateways and development tools. Unlike DOS, OS/2 supported LANs almost from day one with the LAN Manager. LAN Manager's performance is, even in its first version, on a par with older, more refined network operating systems. Also, it lacks their drawbacks, namely, alien file systems and the continual worries about, "Will this work with the next version of DOS?"

Some of the old favorites, like Crosstalk XVI, aren't out yet for OS/2. However, there is no shortage of basic asynchronous programs, like Hilgraeve's HyperAccess/5. Logistique LMM has offered its shareware Procomm-like Logicomm for over a year now, and it's my communications mainstay at the moment—not because of anything lacking from the other packages, but because I learned Logicomm first and haven't had time to explore the alternatives.

Databases are OS/2's first application. R:base System 5 for OS/2 was one of the first, if not the first commercially available OS/2 application. Access to a lot of

continued

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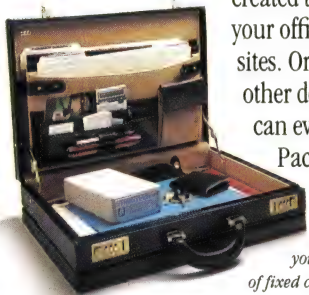


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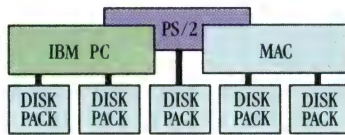


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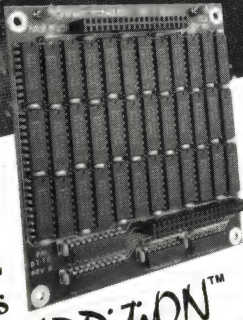
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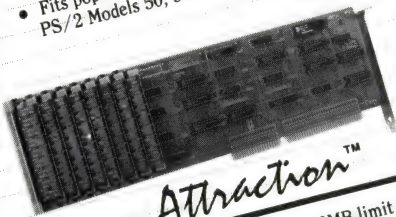
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First, LAN capabilities are built into OS/2. Machine-to-machine communications avenues are right there. Developers needn't mess around with NetBIOS to write LAN-aware applications. Remote execution (another feature built into OS/2) and a machine-to-machine communications system called *named pipes* provide the foundation for client-server-type applications.

Second, OS/2 provides system tools that make multitasking programs easy to create. For example, why should you have to wait while saving a file in a word processor? You should be able to keep working while the save goes on concurrently. This can be done under DOS, but it requires a lot of tricky code. OS/2 has, built in, the notion of *threads* of execution. It's relatively simple to set up a procedure within a program as a separate thread of execution that runs in parallel with the main program. In the word processor case, the "save" thread could save the file in the background while the main editing thread continued. The thread-creation and thread-destruction mechanism is fast, and it involves fairly low overhead.

Third, OS/2's minimum platform is richer than that for DOS. The DOS developer who wants to sell many copies must write a program that will run well on the average user's machine. The average user doesn't have a mouse, so the program shouldn't require one (unless it's a Windows program, which assumes that it's on a platform that requires a mouse). There are several competing video graphics standards, and some video boards don't support graphics at all, so you shouldn't include graphics in a crucial section. Or, if you do support video, you must support all kinds of video—Hercules, CGA, EGA, and VGA at a minimum; AT&T, 3270 PC, 8514/A, and Professional Graphics Adapter in the next bunch; and so on. Ditto color. Very discouraging.

OS/2 eases the burden. The OS/2 developer knows that the target machine essentially *must* have a mouse and *must* have video, and the video is managed by the Presentation Manager (PM), so there's no need to worry about what type it is.

Are OS/2 programs different from DOS programs? Initially, not so much, but the newer applications are showing off OS/2's unique features.

How Not to Write an OS/2 Application

As I said earlier, at this stage in OS/2's history, applications are generally just

continued

O S/2 programs can be fundamentally different from DOS programs.

grams are being moved from VS FORTRAN on IBM mainframes to OS/2, now that the memory to do these applications justice is available. Powerful programs like MACSYMA and Mathematica will no doubt show up in an OS/2 incarnation. Matrix manipulation, linear programming, and statistical packages are all either delivered or on their way. The same programs that you needed a mainframe to use five years ago fit in OS/2's memory space quite nicely.

Every major desktop publishing package will be on OS/2 by the end of the year, as well as a few new ones. And where would desktop machines be without word processing? The two biggies, Word and WordPerfect, are both out in OS/2 versions. And they don't run badly. IBM originally offered the first OS/2 word processor, DisplayWrite 4/2. Now there's DisplayWrite 5/2. Of course, with all this memory and graphics, word processing will continue to look more and more like desktop publishing.

Do OS/2 Applications Differ?

At this stage in OS/2's development, most programs are mere ports of DOS programs. This is, again, a repeat of the DOS experience, where the early DOS programs were ports of CP/M applications. The first dBASE II was indistinguishable from the CP/M version, as were early WordStar and VisiCalc. Ashton-Tate actually shipped the CP/M manual with the first dBASE II.

But OS/2 programs can be fundamentally different from DOS programs, for several reasons:



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DOS conversions. Let's look at an example of how *not* to write an OS/2 application. I don't want to name any names, because the product itself is good enough in its particular product category. Most of the current OS/2 programs share its sins, so I don't want to beat up on it in particular. This application searches for data on a hard disk, akin to what GOf'er does under DOS. It has the ability to search across a fairly wide variety of string patterns.

Under OS/2, this program doesn't seem to have any new functions. Basically, you fill out a request screen that includes the search criteria that you want to use. I can say something like, "Find a line where 'banana' and 'monkey' show up, but not where 'ape' shows up." Then the program starts searching over whatever paths and filenames I tell it to. Very nice.

But the program keeps grinding away, one file at a time. It informs me at the bottom of the screen that it has found, let us say, 30 proper matches. It is still working to find others. Think about that: This program has found 30 files that match my criteria, and it's making me

At this stage, OS/2 applications are generally just DOS conversions.

wait while it looks for others! That's definitely crazy. The edit/display screen should come up immediately with the first match, and the program should then spawn a thread in the background to keep searching.

As the application searches, it comes across a system file, OS2.INI. It gets a "sharing violation." Well, of course it does—that file is kept open by the system. Does it skip over it? No, it actually wants me to answer "Continue or Stop? (C or S)" for every silly open file. On DOS, that's no sweat—there aren't too many open files. But on OS/2? Give me a break. Even if the error *were* legitimate, the program should keep searching other

files while waiting for advice on the problem file.

There are other problems, but you get the picture. Even big-name word processors don't have background saves incorporated yet. DOS-ported programs exploit OS/2 features chiefly in cases where the developer has already labored to add a feature to the application that DOS lacked. The most common one is virtual memory. For example, BRIEF, a text editor under DOS, can edit files that are larger than memory. UnderWare, BRIEF's developer, added extra code to provide the ability to spill file overflow onto a disk. UnderWare happily removed the extra code for the OS/2 version, because virtual memory is an automatic and integral part of OS/2.

The applications that exploit OS/2 features, as would be logical, are those that have been built from scratch under OS/2. Hamilton Laboratories' Hamilton C Shell is an example of this. It makes disk searches seem much faster, for example, by cleverly exploiting multithreading. Since making an application a PM application requires some massive code rewriting, the pile of programs coming in

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for PM will no doubt be built to be more OS/2-aware.

OS/2 Applications Will Appear

Unexpectedly high memory prices and delays from Microsoft and IBM on developer tools have held back OS/2 development. But memory prices are subsiding, and the tools that are out now are fairly good. Third-party debugging products like Logitech's MultiScope are powerful additions to any programmer's toolkit that simplify development.

One reason why OS/2 applications will probably continue to appear is that developers report that once they get started with OS/2, they find that they like it as a development environment. Since it is a protected-mode operating system, applications cannot go too awry without tripping a protection exception that causes the operating system to shut down the errant program. Thus, a not-yet-debugged program won't crash the entire system, only its session, which is then easily restarted.

I've yet to talk to a developer who was dissuaded from working with OS/2 by the quality of the tools. Those who

choose not to write for OS/2 say it's because OS/2 is Intel-specific, whereas Unix is not; OS/2 requires too much (compared to DOS) in terms of hardware platforms; OS/2 is buggy; or OS/2 doesn't use the 80386 features yet, whereas some versions of Unix do.

Like all software, OS/2 will improve with age. Around the time you read this, OS/2 version 1.2 will be released. It will incorporate fixes for things like the brain-damaged print spooler and the lack of printer drivers, as well as introduce the much-improved file system.

Next spring, the 80386 version of OS/2 will finally arrive in version 2.0. That will spur even more software. Remember that the 80286, although blessed with its protected mode that lets it address 16 megabytes of memory, is cursed with having to address it 64K bytes at a time. This is not so with the 80386. It brings a new protected mode, a 32-bit mode that can address 4-gigabyte address spaces, with segments as large as 4 gigabytes. No more fumbling with 64K-byte segments!

There's a lot of software out there sitting on IBM mainframes, VAXes, and

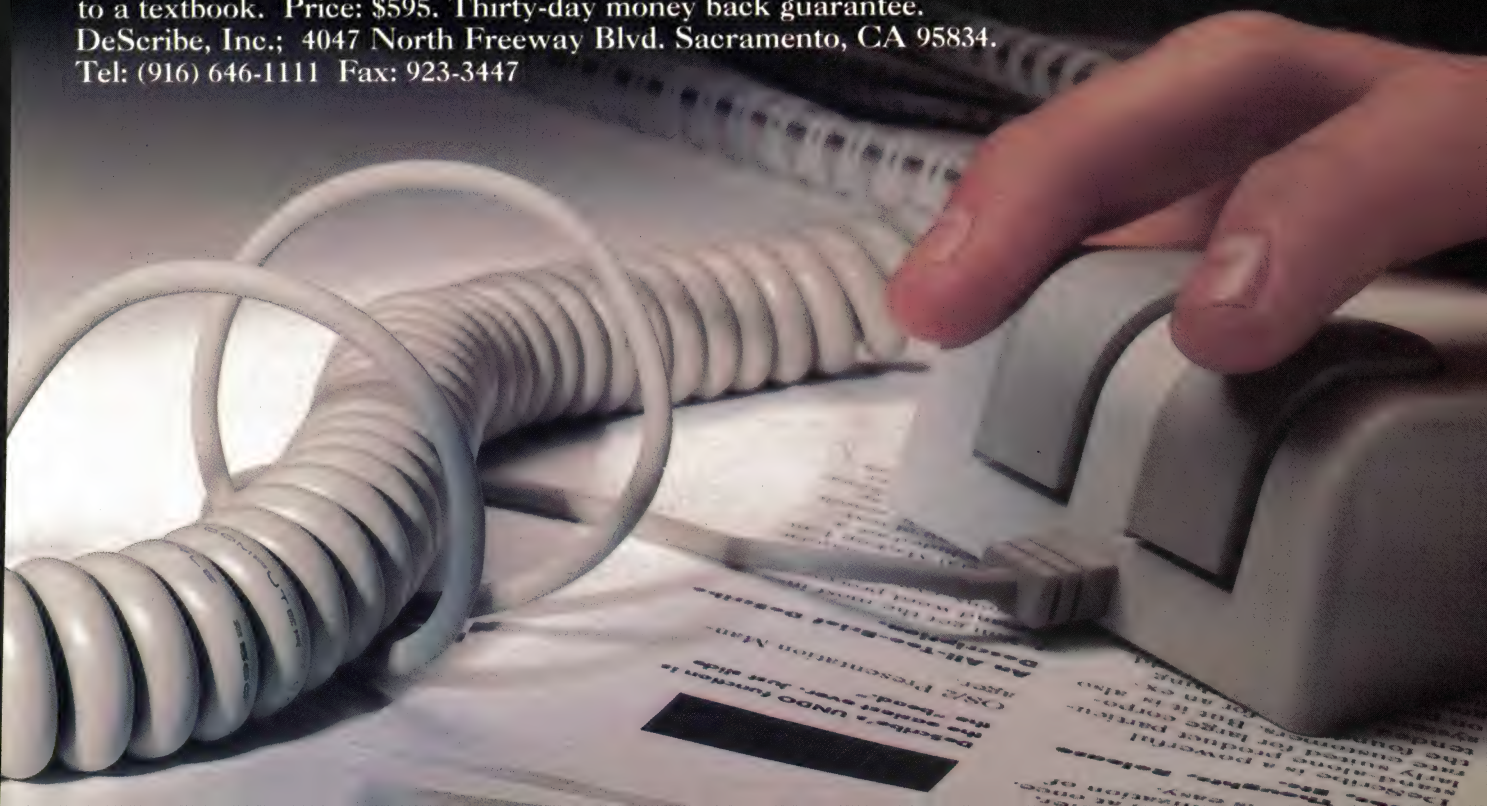
Unix boxes that hasn't been ported to the PC, partly because it's such a pain to cut and arrange everything to fit in the silly small Intel segments. With OS/2 2.0, that problem will go away. The 80386 supports multiple DOS sessions, so version 2.0 can provide the best of both worlds—DOS multitasking and 80386 OS/2 features.

There are hundreds of OS/2 programs in existence today—and thousands more are still to come. Many are warmed-over DOS applications. But native OS/2 programs will appear toward the end of this year and the beginning of next year. Memory prices are dropping, so the largest hardware barrier to OS/2 acceptance is slowly going away. The applications are broad-based and apply to many industries and users. All these things spell success for OS/2—even if not the kind of success that IBM and Microsoft were expecting. ■

Mark J. Minasi is a managing partner at Moulton, Minasi & Company, a Columbia, Maryland, firm specializing in technical seminars. He can be reached on BIX as "mjminasi."

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AIX ON THE PS/2s

*A look at IBM's version of Unix
and why you should care*

Ben Smith

IBM has gone the distance for a qualifying Unix event. It has fully implemented AIX (its licensed version of Unix) on the PS/2s. All the pieces are there, and they all work. But why should you consider using AIX? And for that matter, why should you consider using Unix in any of its incarnations?

Who Wants Unix?

Although there are proprietary operating systems that may offer more capabilities for a specific task, Unix is a generally solid and widely accepted operating system that runs on the widest range of computers in the world. As a result, it offers a consistent kernel around which application programs can be wrapped, giving developers maximum portability for their work.

Unix was developed about 20 years ago at Bell Labs. Since then it has gone through many generations of design and distribution. It became a commercial operating system just before MS-DOS was thrust on the world, but at that time it was generally found only on large minicomputers and mainframes. Now that the microcomputer has grown

to the power and capacity of the mini-computer of five years ago, Unix also is found on the desktop.

Unix utilities and file organization have been the model for the enhancements of MS-DOS. In fact, Microsoft once published a memo to developers that stated that each subsequent release of MS-DOS would bring it closer to Xenix (its license of Unix).

Unix is *not* a reasonable operating system for a single user running a single application program such as Lotus 1-2-3, although it is quite possible to do just that. Unix is a reasonable operating system for a single user doing several tasks concurrently; it is an excellent operating system for many users sharing computing resources and information.

Unix Versions and Politics

Unix goes by many different names (e.g., AUX, AIX, Ultrix, Xenix, and HPUX), but these names all reflect source code licenses from AT&T for roughly the same thing. Each vendor has added its own utilities and enhancements. The basic core and utilities remain the same throughout. Until recently, all the vendor licenses for Unix fell into two flavors, System V and BSD. System V represents the "pure" AT&T release. BSD (Berkeley Software Distribution) is connected with a path of parallel development from the common parent, System 7. BSD was the first version to take advantage of the virtual memory capability of the VAX. Nowadays, all Unix licenses have many BSD features and utilities.

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Recently, AT&T and Sun Microsystems (which is the major exponent of BSD) reached an agreement to codevelop the next release of System V, merging the two versions. But there was a strong negative reaction from many of the manufacturers of hardware for Unix, including Hewlett-Packard, Digital Equipment Corp., and IBM. Although each of these companies had adopted many of the BSD features into their versions of Unix, they believed that the coalition of AT&T and Sun shut them out of the control of the new standards. They decided to form their own standards organization, the Open Software Foundation. All members of this list of elite computer manufacturers contributed huge amounts of money and personnel to form OSF. IBM also contributed the source code of AIX, its enhanced version of Unix.

There is no doubt that AIX will be a major design element in the OSF standard version of Unix. And there is also no doubt that OSF will influence future releases of AT&T versions in the same way that BSD has. Although the union of BSD and System V spawned a new child, OSF, a child often influences the decisions of the parent. AIX will be an important element of design in all future versions of Unix.

AIX

Traditionally, IBM offered Unix only on its RT (RISC technology) machines. But last autumn, it announced that it planned to offer Unix on all families of computers, from its largest (3090-600) down to its smallest, the PS/2s, the first for which it was released. It is shipping, and it is good; but it's also immense. AIX for the PS/2s includes not only all the standard stuff (a selection of shells, editors, mail system, communications, compiler, report generator, calculator, and so on), but also networking protocols (TCP/IP), 3270 support for interfacing with traditional IBM machines, DOS as a guest operating system (Merge), communications with terminal emulation (ATE), and a generous supply of excellent tools for the application program developer.

With all the modules available for PS/2 AIX, there are 50 1.44-megabyte disks. That comes to more than 70 megabytes for the operating system and associated utilities!

Installing an operating system of that size is no small matter. And, if this is your first time, plan on doing it twice. The first installation will serve to ensure that everything works. The second will be necessary to get the disk partitions that you really need. Don't plan on the

second one until you have spent at least a few days experimenting with the first installation. Be sure to spend some of your time with Merge. Decide how much disk space you want to dedicate to pure DOS. Put aside at least 4 hours for each installation. (With experience, you can probably get that down to 2 hours.)

Merge

If you are a DOS user migrating to Unix, you will definitely want Merge (developed by Locus Computing) on your PS/2 AIX. When you run Merge, everything appears as it would when running a vanilla DOS, even though you are actually running AIX as the host and the disk is really a Unix (AIX) file system. Merge manages and maintains DOS files and programs on an AIX partition. (As I mentioned, you may still want a purely DOS partition, though.)

Merge is really the hook in AIX that enables you to run DOS. It is not a DOS emulation like VP/ix (from Interactive Systems). With Merge, you actually install a fully licensed PC-DOS. Disk drives, serial ports, and the screen all behave as if you were running DOS independently of any other operating system. I actually ran System Sleuth from the Merge DOS (see the Short Take "Sleuthing Your Troubles Away," June BYTE). Everything behaved as if there were nothing between DOS and the real physical devices, except when I was memory snooping: There appeared to be only 640K bytes of memory when, in fact, there were 6 megabytes.

DOS is run on a virtual machine, and the devices are managed by Merge and AIX. But your DOS programs will never know: a wonderful and useful illusion. It is so well done that you can easily forget that you are actually running Merge. The stand-alone DOS versus Merge DOS performance degradation is trivial (provided that you have sufficient memory in your system to dedicate 1 megabyte to the virtual machine).

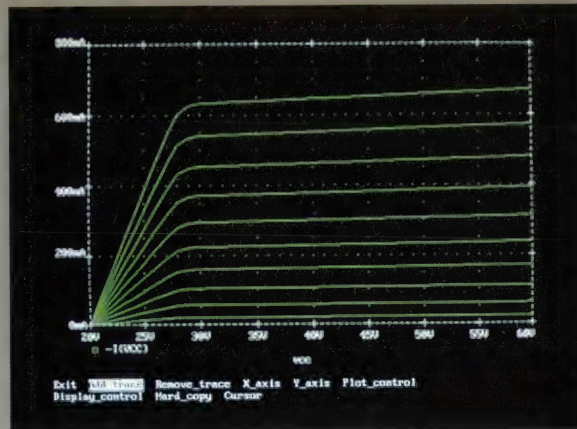
AIX Is Unix

It is nice to have a transition from DOS to Unix, but the real question is, how good is AIX as a Unix? There had been some rumors that AIX was not really Unix. Not true: AIX is real Unix (whatever that might mean). It will be fully POSIX-compliant. (POSIX is the operations specification currently being developed by ANSI and IEEE. It is being supported by the U.S. government and will probably be supported by the International Standards Organization.)

continued

PSpice

The Standard for Circuit Simulation



I-V curves of a triode vacuum tube

Analog Behavioral Modeling

The Analog Behavioral Modeling option for PSpice allows one to describe analog components, or entire circuit blocks, using a formula or a look-up table. For linear blocks, the description can be either a Laplace transform or a table of frequency response. Once defined, PSpice can simulate circuits including such blocks.

The ability to model entire blocks of circuitry is a powerful aid in designing a system from the top down. A functional block can be described by its behavior without worrying about how that function will be implemented. Later, the block can be replaced by the actual circuitry.

Another application is the modeling of electronic components which are not built into PSpice. The photo above shows an example of simulating the DC characteristics of a 3/2-power-law device.

Since its introduction over five years ago, MicroSim's PSpice has more copies sold than all other commercial Spice programs combined. Here are some of the features which have made PSpice so popular:

- Standard parts libraries of over 2200 analog models: diodes, bipolar transistors, small-signal JFET's, power MOSFET's, opamps, voltage comparators, transformer cores, and opto-couplers.
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- Non-linear transformers modeling saturation, hysteresis, and eddy current losses.
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Besides Analog Behavioral Modeling, these other PSpice options are also available:

- **Digital Simulation**, which allows one to simulate mixed analog/digital circuits with feedback between the analog and digital sections.
- **Monte Carlo** analysis to calculate the effect of parameter tolerances on circuit performance. This includes statistical, sensitivity, and worst case analyses.
- **The Probe** "software oscilloscope" provides an interactive viewing environment for simulation results (see photo above).
- **The Parts** parameter extraction program, allowing one to extract a device's model parameters from data sheet information.

PSpice is available on these computers:

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AIX contains all the standard System V calls and utilities as well as most of the Berkeley calls and utilities. Where there are overlaps, Berkeley Unix is given the decision. For instance, ls to the standard output (screen) defaults to a multiple-column list of the file subdirectory. The UUCP (for Unix-to-Unix communications) system is the HoneyDanBer version, BNU (Basic Network Utilities). This more modern set of utilities has more versatile device-control tables and remote-site specific permissions offering better security than the earlier versions found on System V machines. None of the machines using the System V BNU were affected by last year's network worm that brought thousands of computers to a standstill.

The system administration and X Window management programs are IBM's own (more on these later). You will not find EMACS, but vi and its friends are there. The mail system is the Berkeley version. The compiler is IBM's. AIX looks like Unix, feels like Unix, acts like Unix, runs Unix programs, and is a Unix license. It is as solid as any Unix you will find. I have no complaints. In fact, I have many compliments.

Perhaps due in part to shared libraries, but also to good operating-system engineering and compiler design, AIX is faster and more efficient in almost every activity than other versions of Unix on the PS/2s. The only exception is an important one: floating-point operations. Without a math coprocessor, floating-point operations creep along. With the addition of this expensive piece of ceramic and silicon, the floating-point operations are marginally better than their non-AIX counterparts. (I obtained these results with an early version of the new BYTE Unix benchmarks [available on BIX or on disk; see page 3 for details]. Unfortunately, the 25-MHz PS/2 Model 70-A21 that I was using was also an early release, and the machine died before I could complete the benchmarks.)

Special Features

Not the least of my compliments for AIX comes from my gratitude for decent documentation. Although the binding of the documentation is far from elegant, the writing and organization are a considerable improvement over the standard AT&T documents. I have eight full sets of Unix documentation from various sources. The prettiest are Apple's A/UX manuals. But IBM's is the most useful and readable. Most Unix implementers do little more than republish the AT&T

continued



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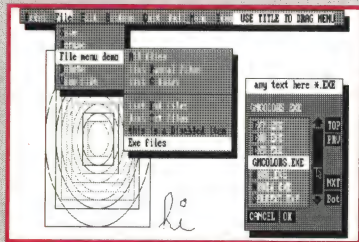
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Table 1: You could spend around \$4000 to become fully involved with AIX.

AIX PRODUCT PRICING

Product	Description	Price
PS/2 AIX	Kernel and basic Unix utilities. 1- to 2-user license included; 1- to 16-user license: add \$200.	\$595
Operating Systems Extensions	UUCP, message handler, mail, and some extensions to system administration and user tools.	\$275
DOS Merge	Hooks to run PC-DOS under AIX.	\$275
Usability Services	Tools and interface for the novice.	\$275
Text Formatting System	Plain ASCII text formatting and typesetting for CAT phototypesetter.	\$220
X Window System	Standard network and local windows communications and controls, including a primitive window manager.	\$214
VS FORTRAN		\$302
VS Pascal		\$302
IBM C Language		\$302
Application Development Toolkit		\$192
Workstation Host Interface Program	Connections to IBM mainframes.	\$441
TCP/IP	Network communications and control.	\$330
Ten/Plus	Interactive Systems' visual shell, editor, and mail system for Unix.	\$275
Total:		\$3998

documents. IBM has completely edited the set and added many useful supplements.

AIX's implementation of Interactive Systems' Ten/Plus user interface is a valuable addition. The core of this is INed, an easy-to-use and aesthetically pleasing integrated file manager and editor. Although it is not as rich in commands as vi nor as flexible as EMACS, it is much easier to learn and allows multiple editing windows. INed provides a history of versions of INed files, from which previous versions can be reconstructed. Unfortunately, in order to provide all these facilities, INed does not use plain ASCII files, although they can be imported and exported. Ten/Plus also includes a mail and remote-connect interface.

IBM has a more general-purpose windowed interface to AIX called Usability Services. I found this interface awkward

and far from intuitive. It can be driven by a mouse, but it requires special Alt-key sequences as well. A good X Window manager and associated user environment would be far more useful than this product.

AIX does provide a solid port of the X Window System (from MIT). Although IBM contributed its own window manager, which provides little more than the public versions from MIT, all the parts are there if you wish to develop your own. I suspect that the AIX window manager is a stopgap until IBM starts shipping Motif (from the OSF), a truly complete graphical user interface and a probable winner on all counts.

Important Subtleties

Of direct importance to the developer and of indirect importance to the end user, AIX implements shared libraries. This means that those parts of different

AIX ON THE PS/2S

programs that are the same are loaded into memory only once. Shared libraries do not become part of the programs until the programs actually run, rather than at the time the programs are compiled and linked. Because a substantial portion of every program is common, shared libraries may use less disk space. Processes that use shared libraries may also require less main memory but may load slower.

As with all modern versions of Unix, the AIX kernel provides some form of virtual memory, the ability to run programs that require more memory than is available in physical RAM. A process running under the kernel uses three standard virtual segments: a text segment (usually the executable code of the program associated with the process), a data segment (the location of most of the variables used by the program), and a stack (the active area used for parameter passing, register snapshots, and address stashing). The use of shared libraries may also specify additional text and data segments. AIX processes can also create and use segments that are shared with other processes.

With the exception of the ugly and unnecessary messages issued from the C compiler that inform you that your compiler is copyrighted by IBM, AIX development tools are excellent, efficient, and well documented. Virtual and shared memory, standardized program message services, program monitor tools, and an advanced symbolic debugger are features that enhance the standard Unix application developer's environment.

Virtual Terminals

AIX provides virtual terminals on the console (the screen and keyboard connected directly to a PS/2). But unlike SCO Xenix and Interactive Systems' Unix, AIX does not use a simple entry in the device directory that looks to the system administration like any other serial terminal connection. Instead, a user already on the system initiates a virtual terminal by issuing open followed by a command. For example, open sh opens a new virtual terminal running the Bourne shell; open dos opens a virtual terminal running DOS; and open login opens a new log-in. There are 17 virtual terminals available. A special key combination rotates through the active virtual terminals. Processes associated with a virtual terminal continue even when that terminal is not being displayed.

Weaknesses

The trend these days is away from stand-alone Unix machines. Networked work-

stations and Unix boxes are the fashion. Although TCP/IP is fully implemented in AIX, the Network File System (developed by Sun Microsystems) is missing, even though it is included in Ultrix (DEC's Unix) and the new System V.4 Unix standard from AT&T. Although NFS is missing, IBM has not been negligent. True to form, IBM is implementing its own network interconnectivity, the Transparent Computing Facility (TCF). (See "A Transparent Environment," July BYTE.) This provides far more utility and transparency than any other comparable system. But it is proprietary to IBM, a great weakness.

Another weak element in AIX for the PS/2s is the system administration interface. Old-time Unix systems required Spartan priests (always a rare class) as system administrators. AIX does provide a more consistent and carefully crafted set of system administration tools than were found in those antique systems. But its set of administrative tools is lackluster when compared to that of SCO and Interactive Systems.

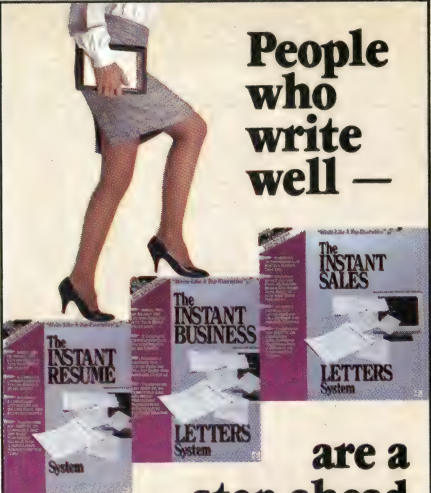
There is no reason that a clever administrator couldn't pull the AIX tools together under a menu structure, but the whole idea is *not* to require a clever administrator. Small Unix systems seldom have more than a few users, none of whom should need to be wizards.

Why AIX on the PS/2s?

The PS/2 configured for AIX is not cheap (see table 1). It is more than twice as expensive as an 80386 AT clone running SCO. So why would anyone want it? And why did IBM develop AIX for the PS/2s? The PS/2 Models 70 and 80 are designed as full 32-bit computers (unlike the AT machines). AIX for the PS/2s takes advantage of the new hardware.

But of greater importance is IBM's commitment to AIX. At first, I questioned the sincerity of its announcement to put AIX on the entire range of its computer families. IBM's demonstration at the 1988 Fall Unix Expo started to build my confidence in the company. IBM has revived its RT line and has nearly completed a full AIX for the 3090. These efforts are encouraging. The implementation of the Locus Operating System as TCF is a great glue to bind together all IBM systems. But the one grain of sand that tipped the scales of belief is the trinket that IBM handed out at the 1989 summer Usenix, a little flashlight with the words, "We've seen the light: AIX." ■

Ben Smith is a BYTE technical editor. He can be reached on BIX as "bensmith."



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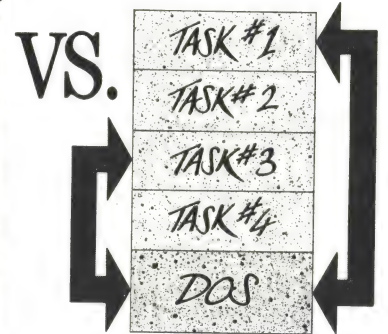
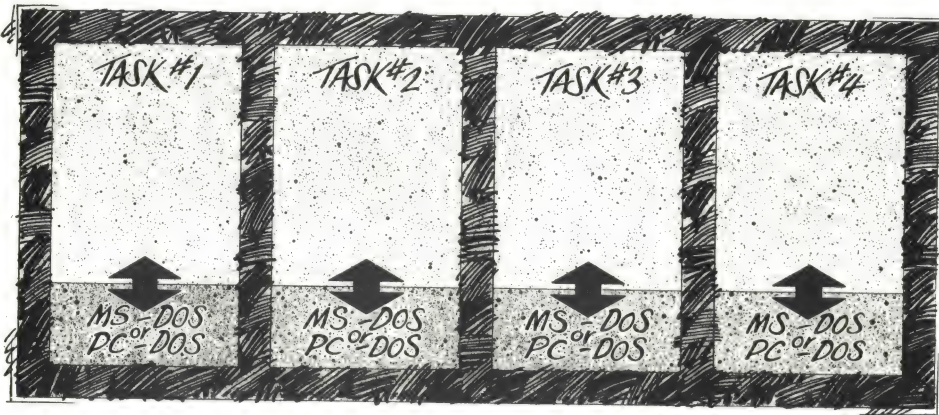
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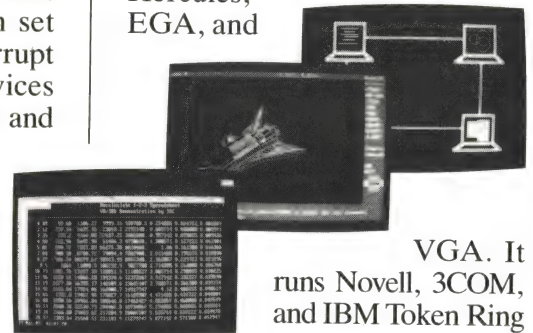
for adjusting the performance and operation of each virtual machine.”

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A host of products bring ease of use to DOS systems without resorting to a graphical user interface

Stan Miastkowski

That bland C> prompt that stares at you from your microcomputer's screen has long been the bane of many new (and even experienced) computer users. Despite all the publicity and excitement about the upcoming generations of graphical user interfaces that will supposedly make computers incredibly easier to use, GUIs are generally designed for high-end (meaning expensive) systems with lots of RAM, fast-access hard disk drives, and high-speed processors. And that's not to mention all the as-yet-undelivered software that has to be fine-tuned to a specific GUI. (For a detailed look at the subject, see "A Guide to GUIs," July BYTE.)

That's all well and good for the future, but if you own one of the millions of low-end microcomputers, you've probably been feeling left out and even forgotten. That's especially true if your system is 8088- or 8086-based, since even low-end DOS GUIs, such as Microsoft Windows and DESQview, either are no longer available for your system or run unacceptably slow. And even if you have an early 6-MHz 80286-based system,

you're still not out of the woods, since these systems often lack the power to handle the large disk space requirements and heavy computational loads that GUIs put on a system.

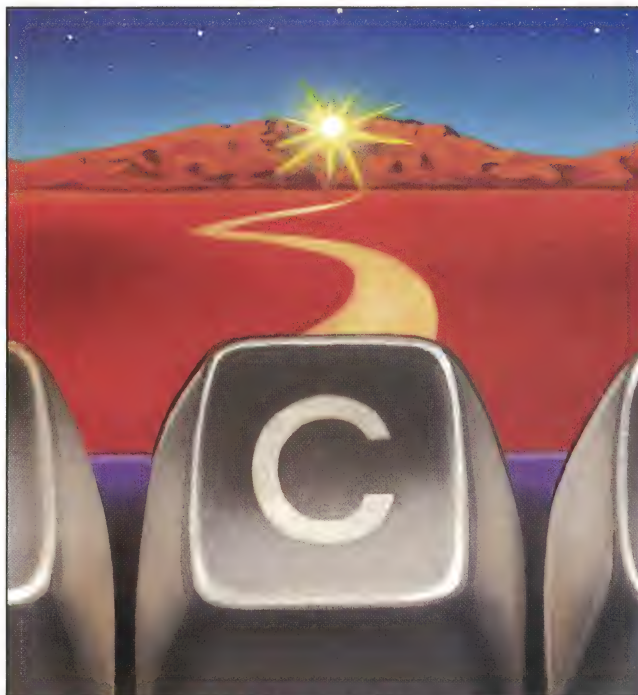
The C> prompt, or DOS prompt, is part of a *command-line interface* (CLI), in which text commands, entered line by line, direct the computer through a sequence of operations. It's actually a lin-

ear descendant of CP/M, the first truly useful and widely available operating system for personal computers. Although the folks at Microsoft would probably deny it, the first version of DOS was a hastily patched-together modification of CP/M concepts (though not the actual operating-system code). In an effort to capitalize on the usefulness of that early operating system, users have been saddled with that C> prompt ever since.

Enter the Shell

As microcomputers became the standard operating platform, it quickly became evident that users needed a better way to interact with their systems. While it usually takes only a straightforward command to start most applications, many users have problems remembering the syntax of even the common DOS "housekeeping" commands (have you ever remembered the precise arguments to format a 720K-byte, 3½-inch floppy disk without looking in a manual?). It only gets worse for those more useful but esoteric commands, such as XCOPY. And there are many things that plain-vanilla DOS just doesn't do well at all. A

continued



case in point is the DIR command, which gives you an unsorted list of files that normally scrolls off the screen before you can find the specific file that you're looking for.

Since hard disk drives are nearly a standard component of most systems, many users quickly build up a large collection of files. And thanks to DOS's "eight plus three" naming limitation (another of CP/M's legacies), filenames often need to be cryptic. DOS's hierar-

chical subdirectory-based file structure is supposed to make things more manageable, but you have to remember which subdirectories contain what data. Even if you remember what goes where, getting there requires that you manually type in a CD (change directory) command, plus the sub-sub-subdirectory name, which makes the whole process a pain. As the amount of information on your hard disk grows, the process of locating and using a specific file gets more time-consuming

and frustrating.

The beginnings of the solution came with what are widely known as DOS shells. Shells are software (usually RAM-resident) that "surround" DOS with a program that interacts directly with DOS's COMMAND.COM. This file, the operating system's command interpreter, intercepts and translates text commands into the low-level system calls that DOS really understands. Another way to think of DOS shells is as integrated environments that sit between your application and the operating system. This extra processing layer extends DOS by adding functions and features that DOS doesn't have by itself.

More than 49 Flavors

DOS shells come in a wide variety of flavors and approaches, but they all have some features in common. Most are very simple file managers: they find, display, and organize files, usually by showing something on the screen beyond that mute C> prompt. That something is usually a list of files in an individual directory, and because plain-vanilla DOS displays files only in the order in which they were put on the disk, shells take the process one step further by sorting them, usually alphabetically. The best shells also give you the ability to sort them by various other parameters, such as size.

A common thread throughout DOS shells is their ability to easily navigate through the maze of subdirectories and files through the simple process of "pointing and shooting." Point to the file (by moving the cursor) and press Return (or click the mouse), and you're moved directly to it.

Another common feature of DOS shells is their ability to perform common DOS operations on files and subdirectories. Although not all packages contain all these features, with most you can do the following:

- Copy files
- Move files
- View files
- Change file attributes (e.g., read-only, hidden)
- Delete files and subdirectories
- Rename files and subdirectories
- Create files and subdirectories
- Tag multiple files for other operations

The key to the usefulness of DOS shells is their ability to perform most of these operations on more than one file at a time. You perform these tasks without having to physically type in individual

continued

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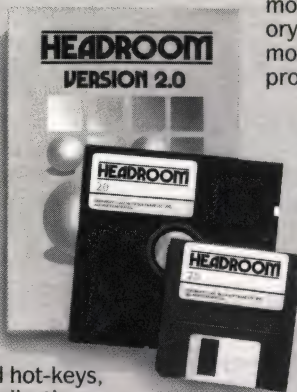
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
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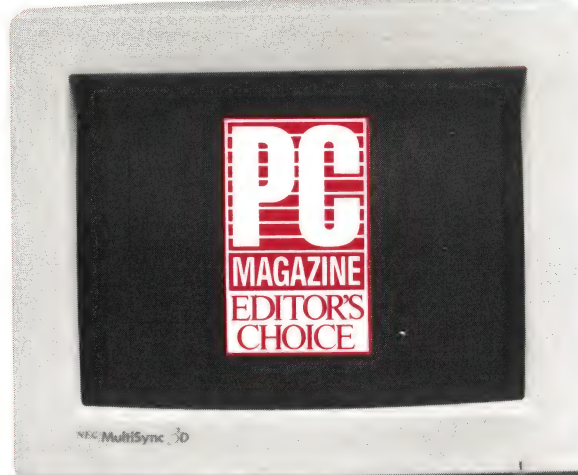
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file or directory names.

Another crucial difference between GUIs and DOS shells is that the shells don't need to be aware of the applications. They'll gladly start any communications file or executable file. That's very different from a true GUI like Microsoft Windows or OS/2's Presentation Manager (PM), where applications must be specifically developed and tailored to the GUI's application programmer interface. Of course, you can run most off-the-shelf DOS applications with GUIs, but only through the pain-in-the-neck process of exiting from the GUI environment.

Memory, Icons, Mice, and Smarts

Until recently, one of the biggest problems with DOS shells was their RAM hunger. Early DOS shells often took up 100K to 200K bytes of precious RAM space. With today's power applications often requiring 512K bytes or even 640K bytes of RAM to run, the RAM requirements of some shells (nearly all of which are RAM-resident) was just too much.

That problem has largely been solved

because the vast majority of DOS shells essentially unload themselves from RAM each time you run an application, leaving a small RAM-resident kernel that "calls back" the full shell when you exit the application. The Norton Commander is a case in point: Normally it takes up 140K bytes of RAM, but it can be configured to leave a small 12K-byte kernel when it's not being used. The DOS 4.0 shell option (described later) does basically the same thing.

Most DOS shells are character-oriented. They don't use those cute little icons, for a number of reasons. One is the simple fact that there are still lots of low-end DOS systems that don't have graphics cards or monitors, and one of the biggest selling points of DOS shells is that they're useful to virtually any DOS user, no matter how limited his or her system.

And with apologies to Macintosh aficionados, the jury is still definitely out on just how useful armies of icons really are. Remembering what a couple dozen cryptic icons actually mean can be as much of a chore as remembering esoteric DOS commands. In fact, GUIs such as Microsoft Windows and OS/2 PM use

very few icons. Instead, they rely mainly on windowing concepts and plain text to get the message across.

Most DOS shells offer additional features for graphics-equipped systems, but icons are still rare, mainly because of the legal questions involved due to the Apple/Microsoft lawsuit. One company that's apparently not too concerned about the legal situation is IBM. Version 1.2 of OS/2 PM (due on dealer shelves by November) will feature many more optional icons, including the ability to design your own. Of course, the ideal situation is to give users a choice of text or icons.

Finally, all the DOS shells mentioned here, from the simplest to the most sophisticated, let you use a mouse if you're rodent-inclined. At the same time, none of them require a mouse. This reflects a still-deep-seated aversion to mouse use in the DOS world. Mouse users and keyboard users still have heated arguments over the relative merits of each method. However, mice are destined to eventually become a near necessity for the easiest access to DOS shell features. All the DOS shells I've used are easier and faster

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to use with a mouse.

Recent DOS shells have become increasingly sophisticated. The crying need for an easier way to interact with DOS has spawned a new category of *intelligent* DOS shells. In addition to file management, intelligent shells can provide you with services based on a file's

characteristics. They let you organize your data by function and context, and they essentially don't care what directory the data is located in. For example, you can associate groups of files with a given program (e.g., these files belong to this spreadsheet program), or you can provide the ability to examine the contents of

spreadsheet or database files without having to run a program (commonly known as "viewing").

Forests and Trees

The tree is an aptly named term for a feature that lets you quickly find individual files in the "forest" of files that inhabit the typical hard disk. It's simply a visual—but not necessarily graphical—display of all the files and subdirectories on a hard disk. In fact, the TREE command has been a little-used feature of DOS since version 2.0, when subdirectories first became available. It was little-used for the simple reason that while it showed you the tree structure on your disk, it did little else. You still had to navigate your way through subdirectories by typing the CD command.

The first and still best known program to take the tree concept and actually make it useful was XTree from Executive Systems (now called XTree Co.). Although it has gone through several iterations (XTreePro is now also available for networks and multiple disk volumes), its basic approach to dealing with DOS remains essentially unchanged. XTree's main screen (see photo 1) is a window into your disk's file system, with subdirectories shown in a tree structure. As you move from subdirectory to subdirectory, the files contained in that subdirectory are shown in a box below it. You can then perform those common file operations on one or more files by pointing to the file, pressing Escape, and choosing the operation.

XTree's user interface is useful because of its elegant simplicity. And the product's basic "look and feel" has been copied by a number of competitors, who have added their own changes, additions, and enhancements. Tree86 3.0 from The Aldridge Co., with its window into the file/directory structure, is similar but takes a more contemporary approach to its user interface by using "drop down" menus. Although its features are similar to those of XTree, Tree86's less cluttered display is a closer-to-GUI approach that many users prefer. It also works best with a mouse, although one isn't required.

And for those of you who would like to have DOS-shell power without a huge outlay of bucks, there's a shareware tree-oriented shell called TreeView. From the folks who distribute a popular shareware package called AutoMenu, TreeView has a raft of features; these include the unique ability to display as many as six different directories and drives at the same time.

Photo 1: XTree was the first add-in DOS shell to incorporate the now-familiar graphical tree display of a disk's directory structure.

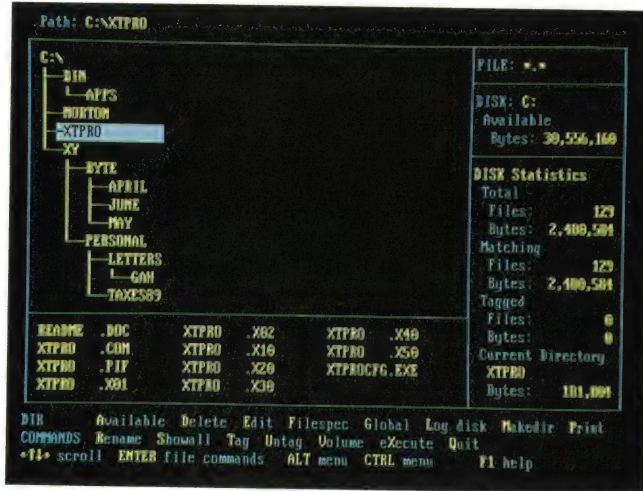
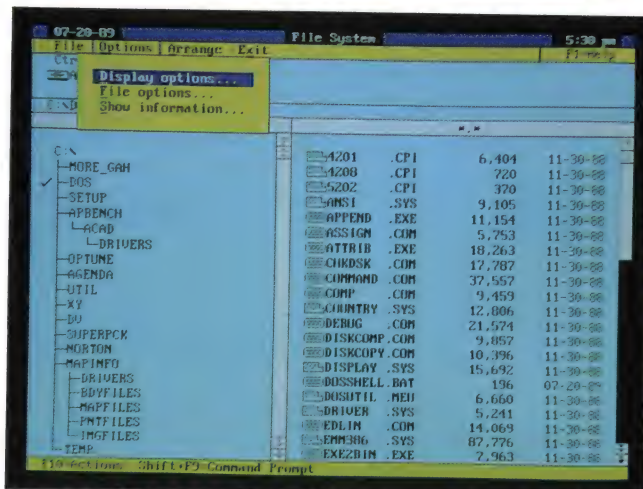


Photo 2: In addition to being the first DOS shell to display multiple directories concurrently, the Norton Commander is the only one that lets you enter DOS commands directly.



Photo 3: The optional shell in DOS 4.0 is IBM's first graphical operating-system interface for PC users. It conforms to the company's Systems Application Architecture.



Letting You Be You

There is one big problem with most DOS shells: While they make dealing with the inadequacies and idiosyncrasies of DOS easier, they often add their own idiosyncrasies that you have to learn to live with if you use them. Like all applications, a DOS shell is one person's (or a committee's) vision of what the DOS interface should be. Although the major packages that I'm talking about here usually have a wide-enough variety of features, some DOS shells are incredibly quirky, seemingly designed by a programmer from another dimension. As with all software, it's best to try before you buy.

One of the most popular DOS shells gives you a choice in the matter. The Norton Commander, now in version 2.0, offers you what at first glance is an incredibly cluttered screen. But the usefulness and organization of what's there becomes apparent quickly. And if you look carefully at the bottom of the screen (see photo 2), you'll see the C > prompt innocently sitting there. If you're an experienced DOS user, sometimes you actually want to bypass shell features and type in a normal DOS command. The Norton Commander is the only DOS shell that lets you do this, and it's indicative of the careful design and hard thinking about user needs that the company puts into all its products.

The Commander was also the first DOS shell that recognized the real-world need to work with more than one directory at a time. Its "dual-window" approach also remains unique to DOS shells and makes the process of copying or moving files from directory to directory or from disk to disk particularly easy, because you immediately see the results of the operation.

Surprisingly, the Norton Commander didn't add a tree display to its list of features until its second release, and then it did so only because Norton Commander users asked for it. Norton's tree display is optional, and most users find that they really don't need it because of the Commander's screen display and the ease with which you can move among files and subdirectories.

Norton also was the first to add advanced file-finding features, and version 2.0 was the first DOS shell to offer *contextual file viewers*. These allow users to view Lotus 1-2-3 and dBASE files as they actually appear in the programs without having to actually start up the associated program. File viewers are one of the most important add-on DOS features to come down the pike in years, and they play a crucial role in the utility of the new

breed of intelligent DOS shells.

The Norton Commander sits squarely in the middle between standard DOS shells and intelligent shells. In fact, you might call it "semi-intelligent." Taking a look at the work behind it also indicates that developing a truly useful DOS shell is far from a trivial exercise. The source code for the Norton Commander 2.0, for example, consists of some 32,000 lines of C and about 15,000 lines of assembly language.

At Long Last, DOS

With the release of DOS 4.0 last year, both IBM and Microsoft finally recognized the need to make DOS easier to use. DOS 4.0's optional SHELL utility bears similarities to the GUI of Microsoft Windows and IBM's PM, with pull-down and pop-up menus.

That IBM included a shell in DOS 4.0 isn't very surprising. It's all in keeping with IBM's commitment to its Systems Application Architecture (SAA), a wide-ranging user interface specification that IBM plans to implement for all its sys-

tems, from mainframes to minicomputers to workstations to microcomputers. The aim is connectivity, and the DOS 4.0 shell is SAA all the way (see photo 3). And because SAA supports both graphics displays and character-oriented displays, even non-graphics-equipped microcomputers can use it. This is, however, a trade-off, because SAA eats into system overhead and runs slowly on many microcomputers.

Unfortunately, there hasn't exactly been a wild rush to DOS 4.0. Part of the reason is that the first release was buggy. And although IBM fixed the bugs in a later release last fall, DOS 4.0 still has an undeserved reputation for incompatibility with older DOS applications and as a RAM hog. But its \$150 price tag, while just a bit higher than many stand-alone DOS shells, also gives you the full DOS operating system.

One particularly even-handed feature of the DOS 4.0 shell is the very fact that it is optional. DOS 4.0 and whatever comes after it are sure to become standards

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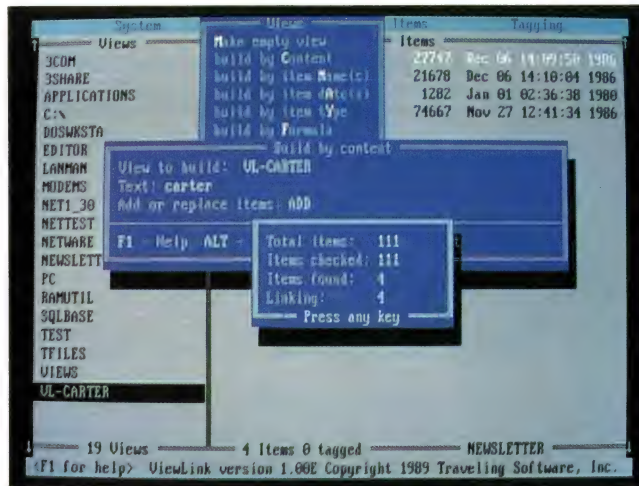


Photo 4: *Traveling Software's ViewLink is the first in a new generation of "intelligent DOS shells," which let you create custom "views" keyed to your style of working.*

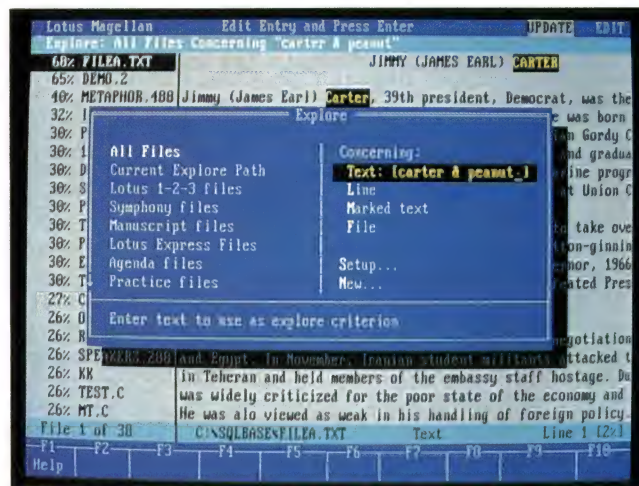


Photo 5: *Magellan uses proprietary technology to index the contents of all files on your disk. It also specializes in performing fuzzy searches.*

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eventually, and it's only a matter of time before developers will take advantage of new features that will require you to use the latest and greatest DOS. But since DOS shells differ so much, there's still going to be a hot market for add-in shells, allowing users to choose the one (if any) that they're most comfortable with.

3-2-1 Launch

Another important part of contemporary DOS shell technology is the user's ability to point to a file and run it. There are two parts to this equation: application files and data files. As mentioned earlier, most shells let you point and shoot at any communications or executable file. Things get more complicated when you want to point to a data file and have it start up its associated application. Macintosh users have had this ability for years, because Mac data files have a header that identifies the applications that created them, but this feature hasn't been available for DOS. That's one area where GUIs shine, but that ability is now slowly becoming available for DOS users.

The Norton Commander and some other DOS shells have a rudimentary ability to associate data files with applications through the simple process of using common file extensions. For example, you can set up the Norton Commander to start up Lotus 1-2-3 every time you choose a filename with a .WK1 extension, or Microsoft Word when you choose a filename ending in .TXT. But true associative file management is only just beginning to become available with intelligent DOS shells.

Adding Real Intelligence to DOS with ViewLink

Perhaps the biggest problem with all the DOS shells I've talked about so far is that they force you to deal with the restrictions of DOS's set-in-cement hierarchical file structure. Although directories and subdirectories make lots of sense internally to DOS, when you stop and think about it, this linear way of working just isn't the way people work in the real world. This is where intelligent shells go a step further by associating data files to their programs.

At first glance, both Traveling Software's ViewLink and Lotus Development's Magellan look a great deal like standard DOS shells, but there's more there than meets the eye. These packages are multifunction software that, in addition to the features of standard DOS shells, incorporate some of the features of indexers, outliners, and even Macintosh HyperCard.

ViewLink links together your data and applications using a concept called *views* (not to be confused with viewing). Views are categories of related data. The crucial concept of ViewLink is that it lets you gather related data into groups based on your work preferences instead of what DOS forces you into.

ViewLink's screen display (see photo 4) is one of those ubiquitous split-screen views. It has the views (categories) on the left, and files you've associated with the views on the right. Initially, the views are primarily subdirectory names. Because the data files that you incorporate into a view are automatically linked to their associated programs, ViewLink has a Macintosh-like ability to directly start

a program when you select the data file.

But in ViewLink's very power lies a paradox. Getting the most out of ViewLink requires a sizable time investment; there's a lot of work to do beyond the initial automatic installation. To get the most from the program, you have to spend a great deal of time continuously fine-tuning it. Having a sophisticated DOS shell that can adjust itself to the way you work sounds great, but the minus side is that you have to take a hard look at your work habits. You'll eventually have a system that acts like it's a natural extension of you, but it takes a commitment that not everyone is willing to make.

The way ViewLink works is tightly tied to specific applications. The installation utility lists some 60 of the most popular application programs. You tell ViewLink which applications you'll be using, and it then goes through a multi-step process that links data files to views and applications, searching through your entire hard disk. The end result is a master link file that keeps track of views, data files, and the applications they're linked to.

Since Traveling Software has applied for a patent for the linking technology, details on it aren't available. But its sophistication is just a harbinger of what you can expect to see in future intelligent DOS shells. For a hard disk filled with nearly 50 megabytes of programs and data, ViewLink's master link file takes up only about 130K bytes.

Magellan's New World View

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as a whole, creating a master index of all files and their contents. Magellan also uses a proprietary technology that Lotus first used in its HAL AI interface to Lotus 1-2-3. Although HAL was a commercial flop, the technology behind it lives on. The Magellan index, which is the key to its incredibly fast performance, creates an index file that normally takes up only 5 percent to 10 percent of the data space. In hopes of making Magellan something of an "industry standard" DOS shell, Lotus has just released the Magellan Viewer Toolkit (\$150). Designed for applications developers, it lets them integrate a Magellan viewer into their finished software.

The most unusual feature of Magellan is its use of custom viewers for popular applications (see photo 5). It goes beyond the limited file-viewing abilities of the Norton Commander. Magellan's integrated viewing technology lets you quickly scroll through lists of files and see most files as you'd see them within the application. Magellan comes with 16 viewers that are automatically invoked, because the files and applications are linked to the correct viewers during the installation process. Magellan even lets you peek into binary files and shows certain packed files (.ARC) in their unpacked state—instantly.

Magellan's index also links data files and applications for quick launching. And its other features are numerous, including the ability to do fuzzy searches using plain-English phrases in an "explore" function. This is DOS shell technology taken to its current limits.

Hope for the GUI-Deprived

Although all the attention of computer buyers seems focused these days on high-end systems and which GUI to choose (when, of course, they become generally available), the continued proliferation of products that enhance and extend plain-vanilla DOS and make it easier to use portends well for the numerous non-power users of nonpower systems. And even many power users will find enough features in these products to decide to stay with DOS until they're compelled to make the substantial investment in the hardware and software for advanced systems like OS/2. The reports of the death of DOS are greatly exaggerated. ■

Stan Miastkowski is a BYTE consulting editor, managing director of K+S Concepts (a documentation and consulting firm), and editor of the OS Report newsletter. He can be reached on BIX as "stanm."

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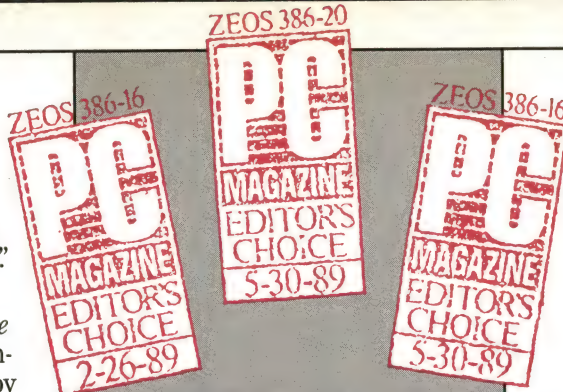
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David M. Yancich

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The 80x86 processors, operating in real mode, have physical addressability to 1 megabyte of memory. Although the 80286 and 80386 processors have greater physical addressing capabilities when operating in OS/2 protected mode, when running in real mode they have the same 1-megabyte limitation. EMS was developed to allow real-mode processing to have access to additional memory. It uses a

technique called *paging*, or *bank switching*. Simply put, paging redirects memory accesses within a 64K-byte, or larger, window of the 1-megabyte physical address space to memory outside of that space. The requirements for expanded memory include additional hardware (in the form of bank-switching registers) and a software device driver. The bank-switching registers

act as gateways between the "physical" window within the 1-megabyte space and the "logical" memory that resides on the expanded memory board. The device driver, called the *expanded memory manager* (EMM), controls the registers so that a program's memory accesses can be redirected throughout the entire range of available expanded memory. The physical address window consists of a

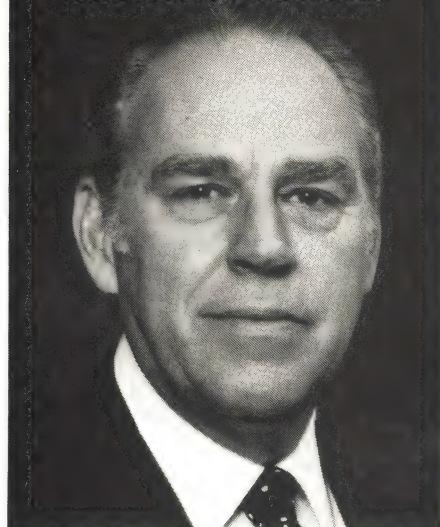
minimum of 64K bytes of unused contiguous memory-address space, accessible in four 16K-byte pages. Each page can be individually addressed and directed to any part of the expanded memory, which is also accessible in 16K-byte pages (see figure 1).

A program that has not been written specifically to take advantage of expanded memory will gain no benefit from it, no matter how much expanded memory you have in your system. To access expanded memory, a program needs to communicate with the EMM for the purposes of verifying hardware/software functionality, allocating memory, "mapping" physical pages with logical pages so that memory accesses are routed to the proper place, and deallocating expanded

continued



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memory when you end the program. Communication with the EMM is similar to making calls to DOS. The program sets up the proper CPU registers and makes a software interrupt request (interrupt vector 0x67). More than 30 major functions are defined by the LIM/EEMS standard, and they give applications and operating systems control over expanded memory.

When a program allocates expanded memory pages, the EMM returns a handle to the requesting program. This handle (integer value) is then used in future calls to the EMM to identify which block of logical pages is being manipulated.

Developing a C Library

Many of the programs that I have written have been for real-time data acquisition and data analysis, applications that require substantial data buffer and data array sizes. Storing this data in expanded memory allows me to generate more code to increase program functionality and user friendliness.

I have developed and placed in the public domain a library for use with Microsoft C that has functions that dynamically allocate and access expanded memory, similar to C's intrinsic malloc() functions. There are several issues that should be considered when developing code that will access expanded

memory, and I will suggest some techniques that may be of interest.

First, you need the low-level functions that allow the application code to communicate with the EMM. The EMM is accessed using software interrupt 0x67. Most C compilers have functions that execute software interrupts. Microsoft C includes several variations, of which int86() and int86x() provide all the proper register passing required to execute the EMM (see listing 1). The functions I will describe were developed using this method. So, while developing these functions is essential to all subsequent steps, the work has largely been done. Complete details of the EMM functions are available from Intel (EMS) and AST Research (EEMS).

When I was writing my programs, I wanted to allocate expanded memory in a manner similar to allocating standard memory using the malloc() functions. I therefore needed a function that would check for memory availability, allocate the desired number of pages, and return some type of information to inform the program of the results. But unlike with malloc(), more information than an address would be necessary. The function, which I call xpmalloc(), returns a pointer to a structure that contains the information shown in listing 2. As with

continued

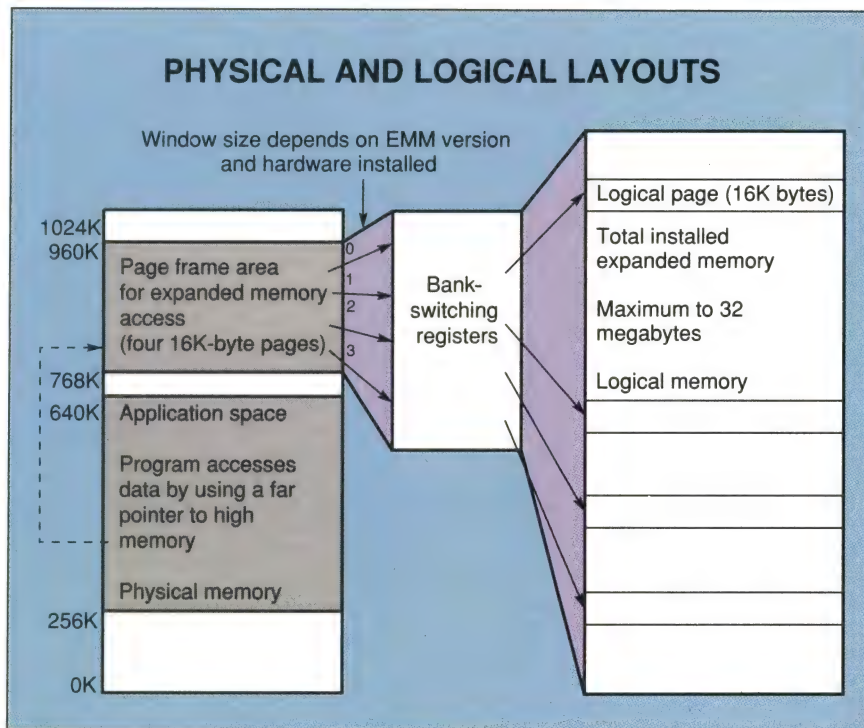


Figure 1: Bank-switching registers direct data traffic between physical and logical memory areas.

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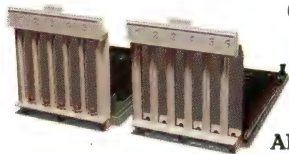
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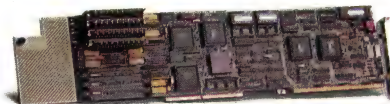
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Listing 1: Low-level functions like this one allow communication between applications and the expanded memory manager.

```
(Get Status - function 1)

#include <dos.h>

#define IAH      inRegs.h.ah
#define OAH      outRegs.h.ah
#define XPMINT  0x67
#define GETSTATUS 0x40

union REGS inRegs,outRegs;

int getStatus()
{
    IAH = GETSTATUS;
    int86(XPMINT,&inRegs,&outRegs);

    return(OAH);
}
```

standard memory allocations, the requested amount of expanded memory is reserved by calling this function, but access requires slightly more preparation.

The next issue to consider is the size of your largest memory allocations and accesses. There are two possibilities: sizes greater than the physical window size (64K bytes) and sizes less than 64K bytes. To access expanded memory, the physical and logical pages first have to be mapped. Since the size of the physical window is 64K bytes, access to data elements greater than that requires new logical pages to be mapped into the window space.

From a programming aspect, this re-

quires that the index into the data be constantly monitored so that if it crosses the 64K-byte boundary, the proper page remapping can occur. If the data size is less than 64K bytes, this is not a concern. As four 16K-byte pages can be mapped at a single time, direct access to 64K-byte memory can occur without the need to remap pages. Obviously, there is a trade-off between performance and array size.

I decided to develop two functions that would take care of page mapping and boundary checking when used with data arrays larger than 64K bytes: one for reading data, and one for writing data. The parameters passed to these functions are the data item index, the data value (writing) or pointer-to-data variable (reading), and a pointer to the `xpmalloc` structure, which was returned by `xpmalloc()`. The values in the `xpmalloc` structure are used in the boundary-checking algorithms and page-mapping procedures.

The functions must be defined for a specific data type so that an element size is known. For example, if the data is to be an array of float, the functions would use $(\text{sizeof(float)} * \text{index})$ to determine if the 64K-byte boundary has been crossed. If the boundary is crossed, new logical pages must be mapped into the physical window.

The next starting logical page number can be calculated by $((\text{sizeof(float)} * \text{index}) / \text{PAGESIZE})$, where `PAGESIZE` = 16K bytes. This new logical page, and all higher logical pages allocated to this array, are then mapped into the physical window, allowing access to data elements beyond the 64K-byte boundary.

It's important to be aware of how page remapping changes the effective index into the data array. Since the physical window consists of 64K bytes of contiguous address space, a conventional memory access for element $(64K \text{ bytes} / \text{sizeof(element)}) + 1$ would have an address that points outside the physical window. Because the new logical page was mapped into the window starting at the first physical page, the effective index for that element is 0 (see figure 2).

My data-accessing functions use a simple mod operation $(\text{index} \% 64K \text{ bytes})$ to calculate the proper physical address associated with the passed index parameter. When programs use these functions, every data access is checked for boundary integrity, causing a performance penalty. However, if the data array must be larger than 64K bytes and the application needs to access the entire array in a random order, the trade-off

continued

Listing 2: Expanded memory is allocated using a variant of the `malloc()` functions. The function `xpmalloc()` returns a pointer that contains memory-allocation information.

```
typedef struct typxpmalloc {
    char *dataPtr; /* Pointer to data (pageFrame) */
    struct tyhandlepages {
        unsigned int handle; /* Expanded memory handle */
        unsigned int pagesAllocated; /* Number of pages allocated */
    } xpmId;
    unsigned int topLogicalPage; /* First logical page mapped */
    unsigned long totalSize; /* Total memory required */
    unsigned int accessedFlag; /* Structure mapped flag */
} typXPMMALLOC;
```

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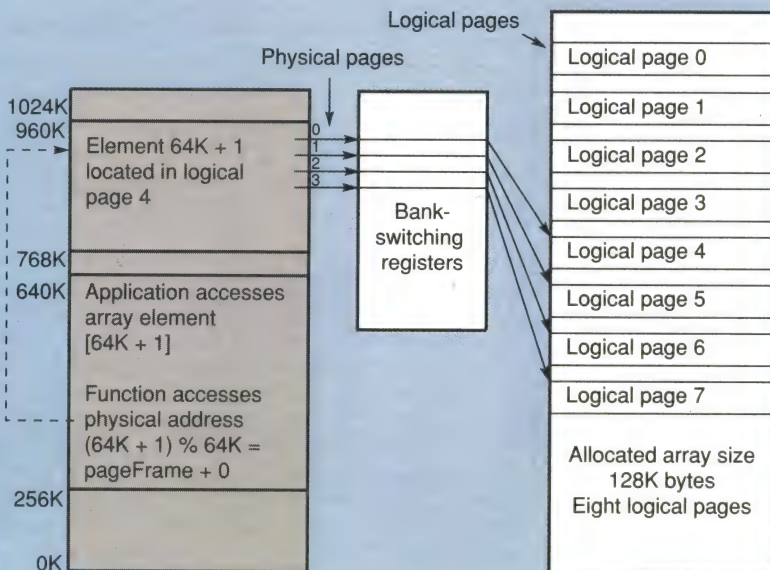
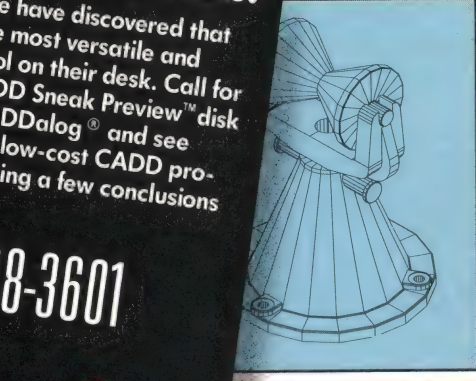
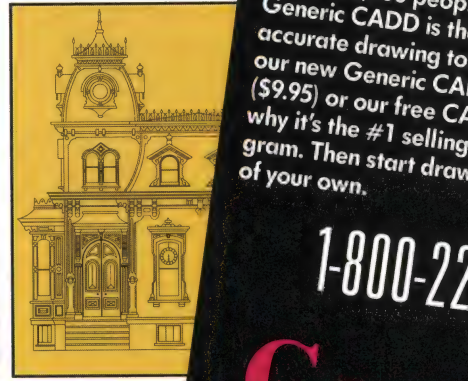
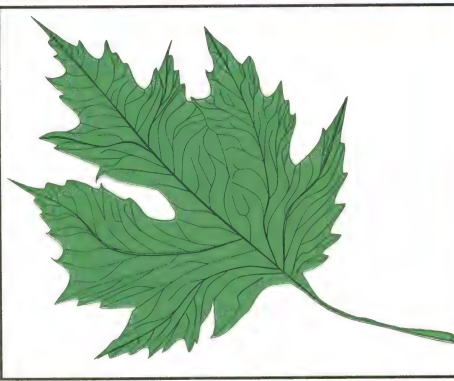
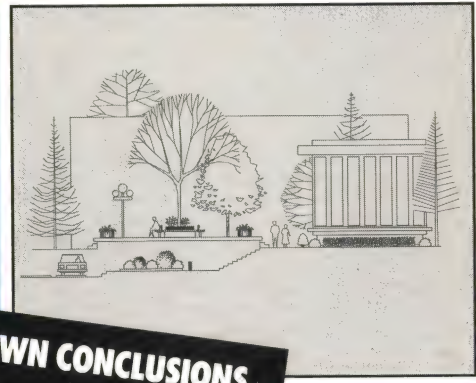
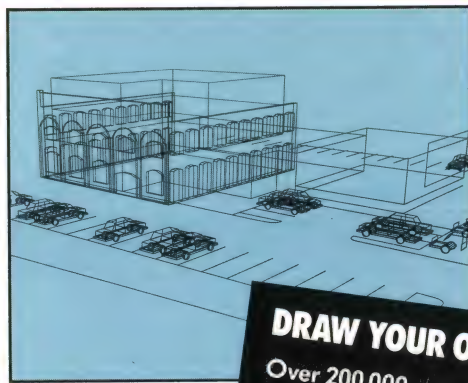
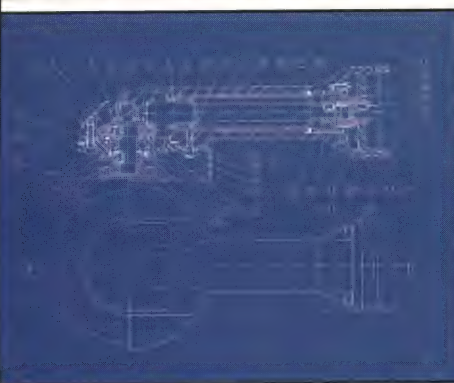
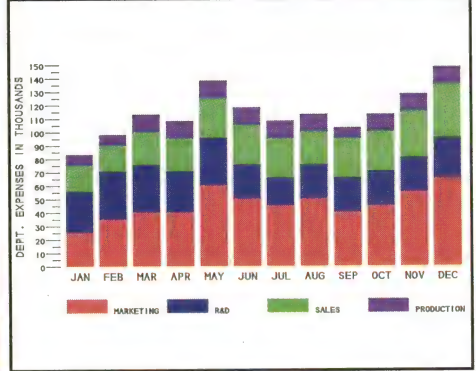
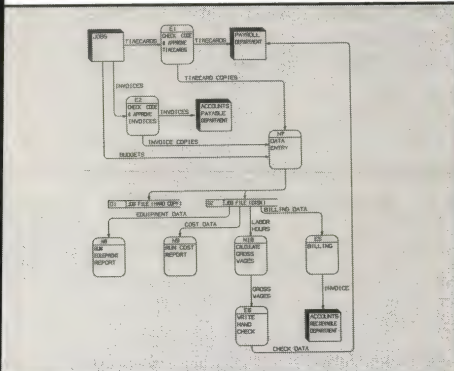
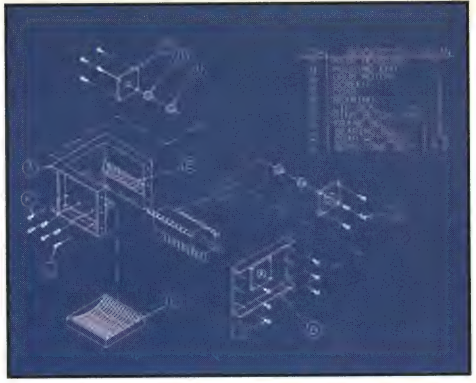
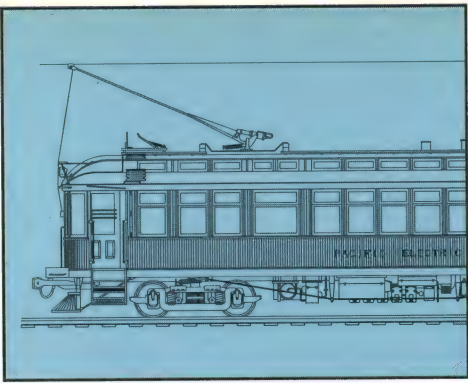
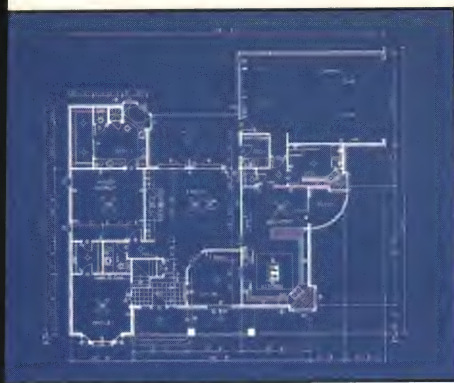


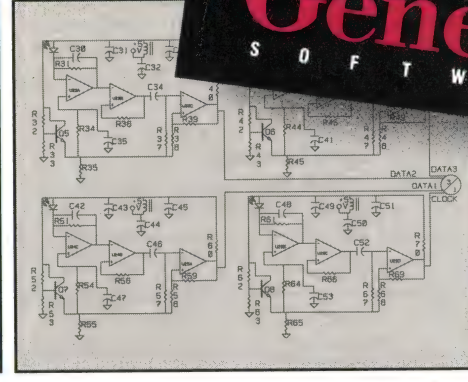
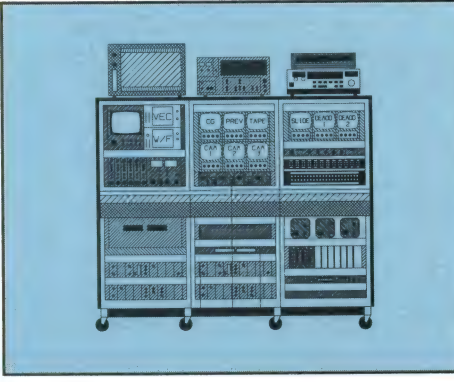
Figure 2: A conventional memory access for element $(64K \text{ bytes} / \text{sizeof}(\text{element})) + 1$ would have an address that points outside the physical window.



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Listing 3: Allocating and accessing a 32K-byte integer array (within the physical window size limit—extended-memory-manager functions assumed available).

```

Initialize
.
.
.
/*
** Code to access expanded memory.
*/
register int i;
int *intArray;
char *pageFrame;
int numOfPages;
int total,available;
int handle;

/*
** 32K array / 16K PAGESIZE
*/
numOfPages = 2;

/* Function 3
** Check for available pages
** returns: total pages and
    available pages
*/
numAvailPages(&total,&available)

/*If there are available pages */
if (available > numOfPages)
{
    /* Function 4
    ** Reserve expanded memory pages
    ** returns: expanded memory handle
    */
    allocatePages(numOfPages,&handle);
}

/* Function 2
** Get pageFrame address
** returns: segment address of
    physical window
*/
getPageFrameAddr(&pageFrame);

/*
** Integer array address will be
** address of EMM window (pageFrame)
*/
intPtr = (int *)pageFrame;

/*
** Function 5 - map individual pages
** Point to proper logical pages
*/
for (i=0;i<2;i++)
{
    physicalPageNum = 1;
    logicalPageNum = 1;
    mapPage(physicalPageNum,
        logicalPageNum,handle);
}

/*
** Access data
*/
for (i=0;i<1000;i++)
{
    *intPtr++ = i;
    - OR -
    intPtr[i] = i;
}

.
.
.
/*
** Function 6 - Deallocate pages
** Release allocated pages
*/
releasePages(handle);

```

favors the boundary-checking function.

When you use expanded memory allocations with third-party memory functions, remember that these functions expect to have access to contiguous addresses. No logical page mapping can be performed externally. Thus, access is strictly limited to physical window size.

Again, in cases where the size of the data is less than 64K bytes, you don't have to do any boundary checking. All required pages can be mapped, and access can occur. Limiting data sizes to the window size is the most straightforward way to access expanded memory. Listing 3 shows an example of allocating and accessing a 32K-byte integer array (within the physical window size limit, with the EMM functions assumed available).

Allowing multiple data allocations has an effect on the page mapping. If only one data allocation is involved, and it is less than 64K bytes, you can map the pages once and forget about them without incurring any further performance penalty. Clearly, this is the simplest and most direct access of expanded memory.

If multiple allocations are involved, and their sizes are less than 64K bytes, logical pages should be mapped before access and unmapped after access (unmapping protects the data from inadvertent accesses). This creates a performance penalty when random accesses to different arrays are required. To reduce this penalty, as many continuous accesses to a single array as possible should be performed before the pages are remapped for a different array access. If both size and multiple allocations are involved, you incur the greatest penalty from the combination of boundary checks and page mapping.

The `xpmalloc` structure includes an integer member, `accessedFlag`, that indicates which data allocation is currently mapped. If the same array is accessed several times in a row, the check for this flag will reduce page mappings and improve performance. Another point to remember when you're allocating expanded memory is deallocation. When your program terminates, all allocated logical pages must be deallocated, or they will be inaccessible for future use until the system is rebooted.

Specific Specifications

The latest expanded memory specifications are EMS 4.0 and EEMS 3.2. These two versions offer several benefits that greatly enhance their use. The major enhancement to both specifications over earlier versions is the ability to have larger physical address windows. This

removes the 64K-byte direct-data-access limitation and allows direct access up to the window size.

The window size will vary from system to system, depending on the amount of unused contiguous address space. Access to a larger window cannot be accomplished by installation of the later version of the EMM alone; an expanded memory board that supports larger windows (i.e., has more bank-switching registers) is also required. Use EMS function 25 (Get mappable physical address array) or EEMS function 33 (Get standard physical window array) to determine the maximum window size that is available in your system.

Along with larger windows in high memory (above 640K bytes), mapping into conventional memory-address space is allowed, but this technique was actually included for operating-system access. Several functions available in the latest versions of the specifications offer enhanced capabilities, such as easy manipulation of memory—both expanded and conventional—and multiple page mapping with a single call.

For example, EMS function 24 provides memory move/exchange capabilities without page mapping. I found this function useful in saving screen images to expanded memory when developing a "windowing" user interface. EMS function 17 will map all pages within the physical window size in one call, which is useful in reducing the performance penalties in page remapping. Some benefits of the latest versions of the specifications require supporting hardware, but some do not. If you have earlier versions of the hardware, you can still install EMM updates and gain some benefits.

The expanded memory specifications have been around for several years, but until recently their use has seemed something of a black art known only to major application or operating-system developers. Today, many well-known and not-so-well-known applications have begun to exploit expanded memory and the EMM functions. If your application is knocking on the 640K-byte door, before you decide to move to OS/2 or other operating systems, give expanded memory a look. ■


Editor's note: *Source code in C for the memory-allocation functions library is available on disk and on BIX. See page 3 for details.*

David M. Yancich is a systems consultant in Baltimore. He can be contacted on BIX c/o "editors."

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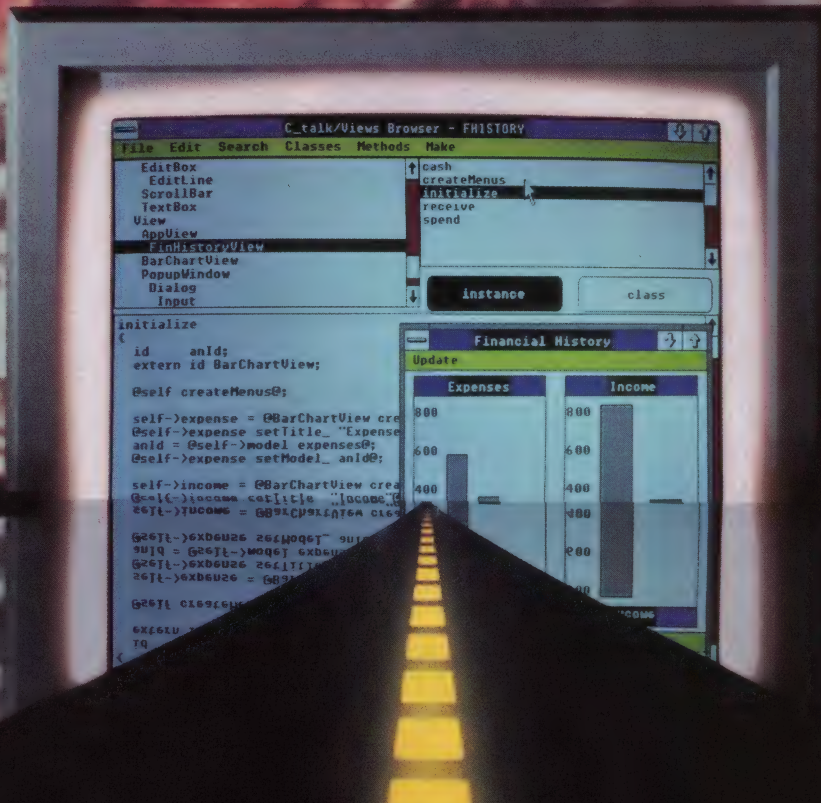
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SERVING MANY MASTERS

New microcomputer bus architectures let multiple devices control input and output in a system

Brian T. Anderson and Marcy A. Puhnaty

Perhaps the biggest performance bottleneck in a microcomputer is the I/O bus. In most machines, the CPU must handle data transfers between peripherals and memory. This keeps the CPU from performing its more sophisticated processing chores and therefore degrades system throughput. Recently, however, new I/O architectures have been introduced that allow peripherals to take control of the bus. Called *bus masters*, these intelligent peripherals represent a significant advance in personal computer design.

Processors and Buses

Since the introduction of the IBM PC in 1981, changes in personal computing technology have focused on the CPU and the architecture of the I/O. CPU technology has migrated from the 4.77-MHz 8088/8086 to the 80286, with clock speeds of up to 20 MHz, and now to the 80386, with clock speeds of up to 33 MHz. The next plateau, 80486 technology, is fast approaching. But because a system is only as fast as its slowest part, faster processors alone cannot ensure faster systems. Improvements in I/O technology

are also critical in improving system performance.

The evolution of the I/O bus architecture in microcomputers hasn't been as straightforward as the evolution of CPUs. It is much harder to speed up the bus than it is to speed up the CPU. You do gain some performance benefits by simply speeding up the bus, but you also run the risk of losing compatibility with

existing peripheral devices and applications software.

The Evolving Standard

The most common microcomputer I/O bus architecture is the Industry Standard Architecture. ISA is an 8-MHz bus with 24-bit direct memory access (DMA), providing 16 megabytes of addressable memory. It was introduced with an 8-bit data path by IBM in the XT. The second version, with both an 8-bit and a 16-bit data path, appeared in 1984 in the AT. The ISA bus in the AT is a superset of the ISA bus in the XT, so all peripheral devices compatible with the XT are also compatible with the AT. Billions of dollars have been spent on peripheral devices for this architecture.

The need for an improved PC bus architecture was prompted by the introduction of the 80386 processor. The increase in CPU performance that this chip engendered led IBM to introduce the Micro Channel architecture in 1987 with the PS/2 line of personal computers. MCA is a 10-MHz bus with 24-bit DMA, providing 16 megabytes of addressable memory. It also features a 32-bit data path. MCA is not

continued



compatible with the existing ISA standard and therefore will not support any of the existing ISA peripheral devices.

As an alternative to MCA, microcomputer manufacturers formed a consortium in October 1988 to establish a new bus architecture that would maintain compatibility with the ISA bus while providing for the advanced features introduced by MCA. The result is the Extended Industry Standard Architecture.

EISA is an 8-MHz bus with 32-bit

DMA, providing 4 gigabytes of addressable memory. The consortium—the so-called Gang of Nine—consists of AST Research, Compaq, Epson America, Hewlett-Packard, NEC Information Systems, Ing. C. Olivetti & Co., Tandy, Wyse Technology, and Zenith Data Systems. Intel has announced the availability of the EISA chip set, and EISA machines should be available later this year.

In addition to 32-bit data paths, MCA and EISA both feature notable advances

over ISA. These include switchless auto-configuration, bus mastering, and burst-mode transfer. Of these, bus mastering is the most intriguing and promises the greatest performance benefits over the long term.

Basics of Bus Mastering

Put simply, a bus master is an intelligent device—typically, a microprocessor—that interfaces to the system bus and has the ability to control the transfer of data across that bus without intervention from the CPU. Since the CPU is not used for bus management, the bus master can operate in parallel with the CPU to transfer data across the bus at high speeds. This differs from the standard ISA I/O bus architecture, where the CPU controls all bus activity with the exception of DMA. In the case of DMA, devices that are attached to the bus transfer data directly to main memory using the system's DMA controller instead of the CPU.

All peripheral devices attached to the bus are categorized as either masters or slaves. Whereas a master can take control and own the bus, a slave device must use the CPU to manage all bus transactions. Slave devices are serviced by the CPU only after a request is made via an interrupt signal. This signal notifies the CPU that the slave device needs it and the bus for a transaction. In ISA-based microcomputers, all peripheral devices are slaves; the CPU is the only master.

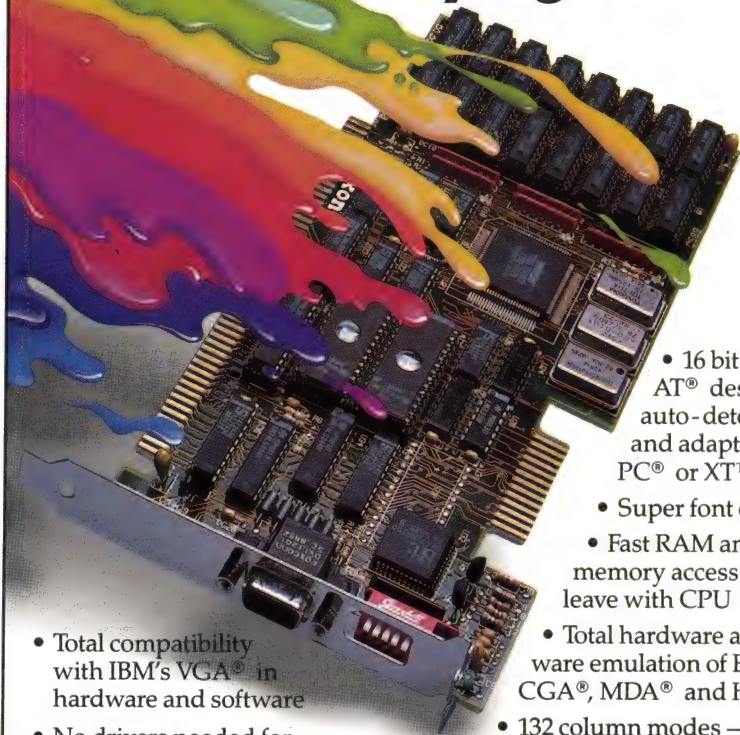
A bus master can play either of two roles in a computer system: It can be dedicated to handling specific tasks, or it can be a general-purpose processor. Typically, task-oriented bus masters are peripheral devices that perform high-performance tasks such as graphics, network control, and data acquisition. General-purpose bus masters are typically coprocessor peripherals. A coprocessor peripheral acts like the CPU so that the system work load can be shared or split between the two.

Sharing Control

A system bus can effectively support multiple bus masters by implementing a bus-arbitration mechanism in the bus-control circuitry. Bus arbitration selects and grants control of the bus to a bus master. When several bus masters are contending for control of the bus at the same time, a central arbiter mediates the requests according to assigned priority levels. Depending on the implementation, priority levels might be assigned according to slot identification number or location, or the priority information

continued

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might be stored on the bus-master board, as in the case of MCA. In this way, no bus master can control the bus for indefinite periods of time.

Bus architectures provide several signals to facilitate bus arbitration. Bus masters use these signals to request control of the bus and to determine if the request has been granted. Although bus-arbitration signals vary across architectures, all perform the same general function. For example, AST Research's SMARTslot architecture provides a very simple approach to bus arbitration. SMARTslot was one of the first ISA-compatible bus architectures to support bus mastering through the use of additional connectors added to the bus slot. Under SMARTslot, each slot has its own dedicated set of bus-arbitration signals: bus request, bus grant, and a shared bus busy signal. To request control of the bus, the bus master sends a request by asserting its unique bus-request line. The bus arbiter on the system board then determines which requesting bus master has the highest priority level. Bus control is then granted to the winning bus master by asserting that board's unique bus-

A
bus master can take complete control of the system bus in order to transfer data to main memory.

grant line. When the bus master detects the bus-grant line, it asserts the bus busy signal to indicate that the bus is in use.

The Mastering Advantage

To assess the relative merits of bus mastering versus standard ISA bus communications, consider how each method transfers data to main memory. With ISA, the CPU controls the entire transaction. First, the CPU performs a read to

the peripheral device to obtain the information to be transferred. It then writes that information to main memory. Thus, the transfer requires two bus cycles: one for the read and one for the write. With a bus master, however, only one bus cycle is needed to transfer the data to main memory, and the CPU is bypassed altogether. With a bus master, only the write operation requires use of the bus. In theory, use of a bus master doubles the data transfer rate for this operation.

Another important advantage of the newer PC I/O bus architectures is the ability of bus masters to perform burst transfers. Burst-mode operation allows a bus master to transfer a block of data during a single arbitration cycle. For example, 16 bytes of data can be transferred in one block using burst mode with MCA, as opposed to just 2 bytes under normal data transfer operations. Because the bus master operating in burst mode is transferring data in larger blocks, it can complete its transfer in less time and relinquish control of the bus faster so it can be used by other system devices. Bus masters initiate burst mode

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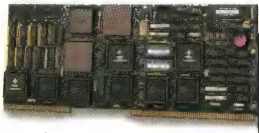


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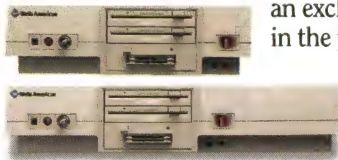
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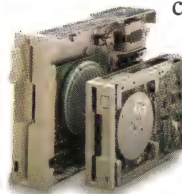
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in different ways. With MCA, for example, bus masters request burst mode via the burst signal on the bus.

Bus-master technology permits a completely open bus. It allows a bus master to take complete control of the system bus in order to transfer data to main memory or to other peripheral devices attached to the bus. For example, communication can occur directly between a bus-master network controller and the system's hard disk-controller interfaced to the system bus. Communication between intelligent devices attached to an ISA-based system can occur only via the central processor. Depending on the bus implementation, the CPU could continue to handle other system tasks while the bus-master device has control of the system bus. Such is the case with MCA. This functionality facilitates multitasking by providing an effective foundation in hardware to distribute processing. Specific tasks normally performed by the CPU can now be off-loaded to the bus master.

To gain a better understanding of the benefits provided by bus mastering and burst-mode transfers, you need to examine the specific implementations of this technology.

Bus Flavors

Bus-master technology is an integral part of numerous bus architectures. In the microcomputer world, you can find hardware support for bus masters on IBM's MCA, AST's SMARTslot architecture, and the NuBus architecture most notably used by Apple's Macintosh II. Machines using the EISA bus, expected late this year, will also support bus-mastering technology. Each of these buses approach the implementation of bus-master technology in different ways to accommodate unique objectives.

Although not a complete implementation, the original ISA has a provision for another bus master aside from the CPU. This feature is implemented by a special signal on the ISA bus called MASTER. A bus master takes control of the ISA bus by first issuing a DMA request (DRQ) to a DMA channel. Upon receiving a DMA acknowledge (DACK), the bus master brings the MASTER line low. It now has complete control of the system address, data, and control lines. Data transfers can now be made without the help of the CPU, thus saving clock cycles.

Since the ISA bus architecture contains no arbitration circuitry in hardware, the mediation of requests between multiple bus masters and the automatic transfer of bus control to an alternate bus

continued

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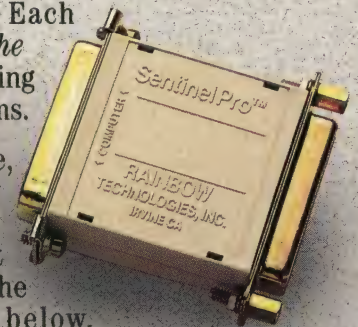
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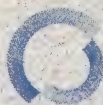
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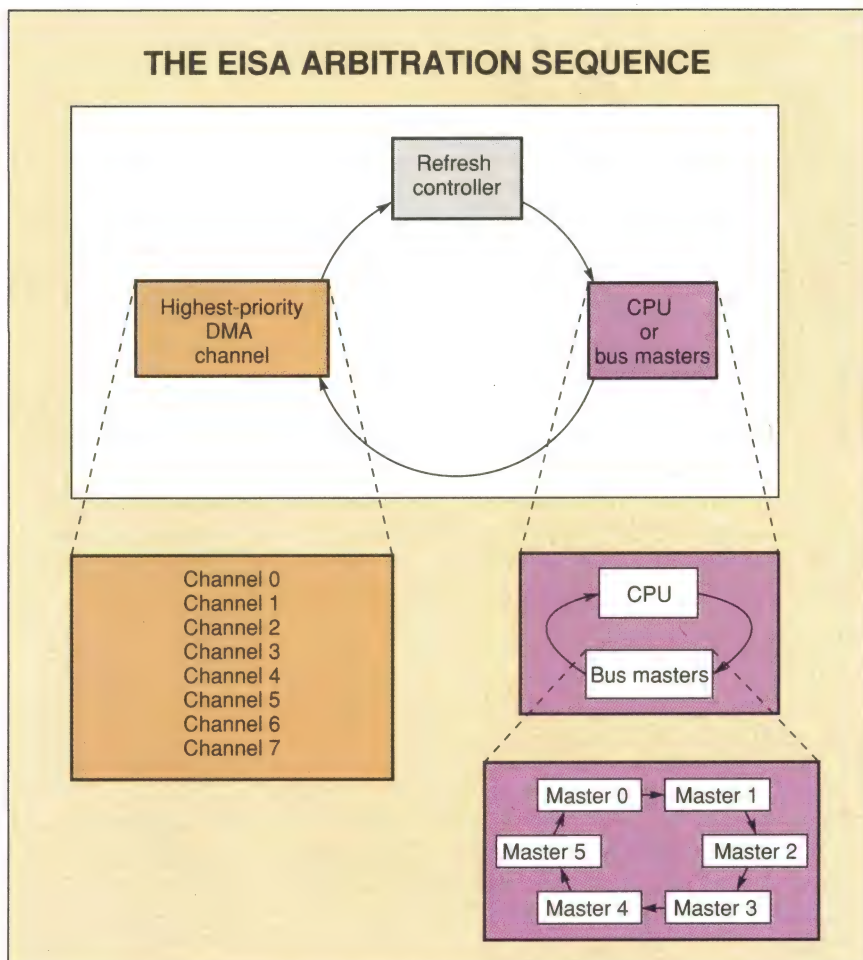


Figure 1: The round-robin priority scheme allows bus masters to gain control of the bus while maintaining compatibility with current ISA direct-memory-access peripherals.

master cannot occur. Therefore, only one bus-master board can reside on the ISA bus. This bus master cannot transfer blocks of data under burst mode, as can MCA or EISA. An ISA bus master is limited to transferring 2 bytes per cycle. The lack of burst mode and the exclusion of bus arbitration on the ISA architecture has inhibited development of boards operating as bus masters for the ISA bus.

The MCA

IBM's MCA extends the CPU's local bus to provide an easy interface to the outside world. In this way, it is quite similar to the ISA bus. MCA, however, has many additional features, including support for bus masters and a 32-bit data path.

Bus arbitration on the MCA is distributed, meaning all contending bus masters play a role in the arbitration process. When a bus master wants to take control of the bus, it first drives the arbitration request signal (PREEMPT). When the

previous bus master is finished with its data transfer, the central arbiter recognizes the PREEMPT line and then drives the arbitrate/grant (ARB/GNT) line into arbitration state. When the ARB/GNT line goes to the arbitration state, the bus master places its priority-level identification into the arbitration cycle on the four arbitration lines: ARB0, ARB1, ARB2, and ARB3. Each bus-master device then monitors these signals. If a bus master detects a priority level higher than its own, it removes itself from the arbitration cycle. At the end of the arbitration cycle, the ARB/GNT line changes state from high to low, thereby granting control of the bus to the bus master with the highest priority.

MCA also supports a fairness feature to prevent higher-priority devices from retaining indefinite control over the bus. It is important to note that priorities for system devices in MCA, such as DMA channels, are fixed in hardware. How-

ever, some of these fixed priorities can be changed through programming. MCA supports up to 16 bus masters.

ISA Extensions

AST Research's SMARTslot architecture is a fully compatible 16-bit ISA bus extended with additional signals to support multiple bus masters. Arbitration control is centralized in the system's bus-control circuitry, and arbitration priority-level assignments are fixed according to slot location. Each slot has its own unique arbitration signals for communicating with the central arbiter. Up to three bus masters are supported in addition to the CPU.

The EISA bus, like SMARTslot, is a fully compatible extension of the ISA bus. It supports multiple bus masters as well as a 32-bit data path, enhanced DMA functions, burst-mode transfers, and switchless auto-configuration. Arbitration on the EISA bus is also centralized on the system's bus controller. Arbitration priority levels are fixed, and each one has its own line to signal requests for bus control on a rotational basis. Figure 1 illustrates the EISA rotational arbitration sequence. Note that a three-way rotation occurs between DMA, DRAM refresh, and all other devices in the arbitration scheme. DMA is given some preference to provide for compatibility with existing ISA DMA devices. It is important to note that although EISA is an open specification, all participating vendors are under nondisclosure on the specifics of the specification until the first EISA machines are released.

NuBus

NuBus is a true arbitrated system bus independent of the CPU. NuBus uses a distributed arbitration protocol like MCA and also supports an arbitration fairness scheme. Once a bus master has been granted control of the bus and subsequently releases it, this bus master cannot arbitrate for the bus again until all other requests have been serviced. NuBus also provides bus and resource locking signals to enhance the use of bus masters for multiprocessing applications.

Bus-Master Peripherals

Although bus mastering is relatively new to personal computers, it has been implemented on some peripherals. Some representative examples follow.

Even though the ISA bus does not efficiently support bus masters, some third-party board makers have designed add-in boards that make use of this feature.

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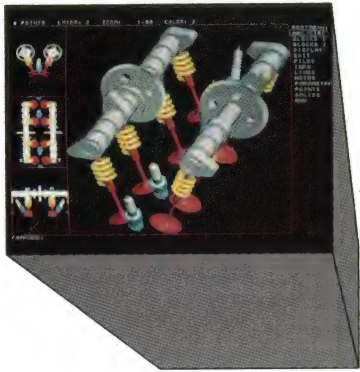
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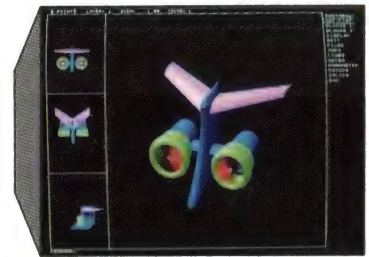
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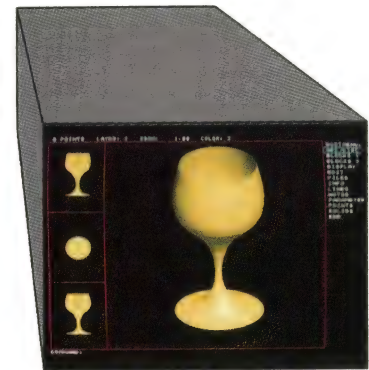
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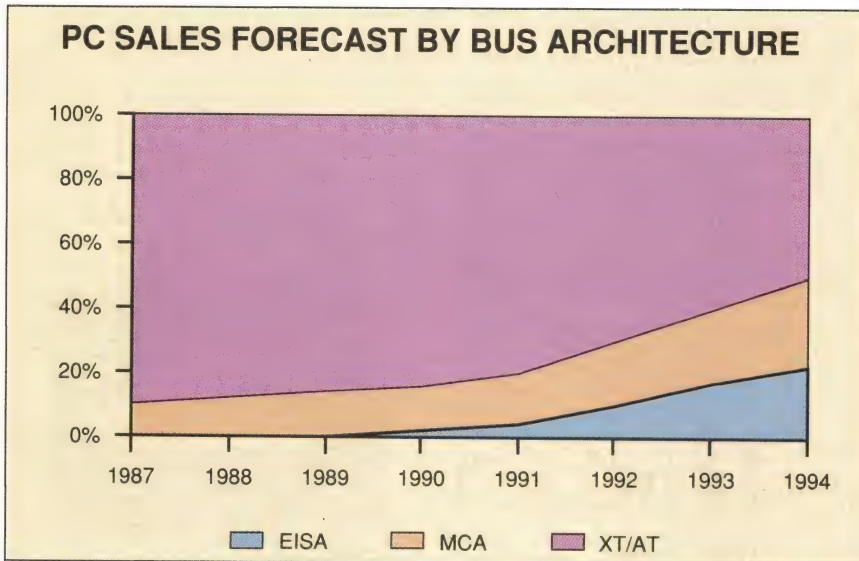


Figure 2: Bus-mastering technologies are expected to account for half of microcomputer sales in 1994. (Source: InfoCorp)

Racet Computes Ltd. (3150 East Birch St., Brea, CA 92621, (714) 579-1725) manufactures the RCP host adapter for SCSI or ESDI subsystems. By implementing the bus-master feature of the ISA bus, the RCP host adapter is capable of transferring data at a minimum of 850K bytes per second across the bus by eliminating the involvement of the CPU in data transfers. The RCP accomplishes bus mastering through the use of firmware on the board and software drivers.

BICC Data Networks (1800 West Park Dr., Westborough, MA 01581, (508) 898-2422) produces the Isolan 4110-3 Ethernet bus-master controller for MCA. The Isolan board is one of the first MCA cards available that takes advantage of bus-master technology. It is unique in that it supports bus mastering without the use of a microprocessor.

According to engineers at BICC, the arbitration control and burst-mode transfers can be effectively implemented using programmable array logic chips and the MCA bus-controller chip on the expansion board. Their MCA Ethernet controller can transfer 16-byte blocks at one time using bus mastering and burst mode, versus the 2-byte maximum on an ISA bus. The board's ability to transfer data in larger blocks allows it to complete its transfers in a shorter period of time. This means that the controller's requirement for bus bandwidth is reduced, and the bus is more frequently available for use by other devices and the CPU.

Ironically, BICC developed its MCA Ethernet bus-master controller before it developed an ISA bus version. Although

the card was designed from scratch specifically for MCA, BICC converted it to act as a bus-master Ethernet controller for the ISA bus.

IBM demonstrated a prototype general-purpose bus-master peripheral device code-named Wizard at Uniform in February. Wizard is an accelerator card that uses the Intel 80860 RISC processor. IBM equipped a PS/2 Model 80 with the Wizard board and OS/2 to compare its performance against the Sun Microsystems Sun-4/110 workstation and the Silicon Graphics Iris-4D workstation. IBM representatives claimed a performance improvement of 30 times that of the Sun workstation and eight times that of the Iris workstation for computational and graphics processing. IBM has also developed a System/370 general-purpose bus-master adapter for its PS/2 computers.

Although IBM is not actively marketing the product, it is available upon request. The System/370 card allows the PS/2s to run System/370 software.

IBM demonstrated a number of task-specific bus-master cards at 1988's Fall Comdex. Among them was a SCSI adapter card that could simultaneously control several SCSI hard disk drives. It was developed by IBM to demonstrate the benefits of bus mastering. IBM also demonstrated Texas Instruments' bus-master Token Ring adapter, which took over most network management duties from the CPU. IBM representatives claim that this technology lets the CPU in a PS/2 operate at 70 percent to 75 percent efficiency, since it will not have to deal with network management chores.

It is very important to note that there have been no formal announcements in the operating-system or applications software arenas with respect to support for bus masters. When available, this support will provide greater increases in system performance than what is provided by hardware alone.

The Road from Here

As is typical in the microcomputer industry, I/O hardware technology is far ahead of available peripheral and software support. Lack of support has limited immediate user demand for the new technology and has created a reluctance on the part of peripheral and software developers to embrace the new I/O bus technologies. Despite this lack of immediate support, bus architecture and bus mastering have become important issues to people making microcomputer purchasing decisions. The reason is that I/O bus technology can greatly affect the longevity of the system you buy.

The new bus technologies are a hardware foundation for the future. As peripheral and software support for the new I/O architectures builds, the benefits of bus mastering and burst transfers will be apparent. Bus mastering provides a way to protect your investment in microcomputer technology while taking advantage of new technologies. In the short term, bus masters will first make a dent in networking, data acquisition, and graphics applications. In turn, these pioneer products will sell more bus-mastering machines, which will lead to the development of more high-performance bus-mastering products. With high-performance peripherals available to free up your CPU, you don't need to constantly upgrade to higher-performing CPUs to upgrade the overall performance of your system.

Bus mastering is the wave of the future (see figure 2). Unlike the ISA bus, it will allow you to migrate to higher levels of performance without having to migrate to a new CPU. This will lengthen the usable lifetime of your microcomputer, thus protecting your investment in today's technology. ■

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CLASH OF THE GRAPHICS TITANS

IBM and Texas Instruments present rival graphics standards

Rick Cook



VGA, the latest graphics standard for MS-DOS- and OS/2-based computers, offers 640- by 480-pixel resolution and 256 available colors. This is much better than earlier graphics standards, but users are already demanding higher resolution and more colorful graphics.

This demand is due in part to the "more-is-more" mentality that has driven the computer industry. Part of it is the need for higher resolutions for specialized applications like CAD and desktop publishing. However, much of the demand is due to the growing appeal of windowing interfaces like Presentation Manager under OS/2 and Microsoft Windows for MS-DOS. Although they can run on lower-resolution monitors, they look much better in high resolution.

Making displays that are much more capable than VGA requires some fundamental changes in the way that MS-DOS and OS/2 graphics systems work. Until now, the standard displays have been based on direct memory access, with the CPU doing most of the work. A display was treated as an area of the

computer's main memory, subject to manipulation by the main processor. However, this gets increasingly clumsy and time-consuming as resolution and the number of colors increase.

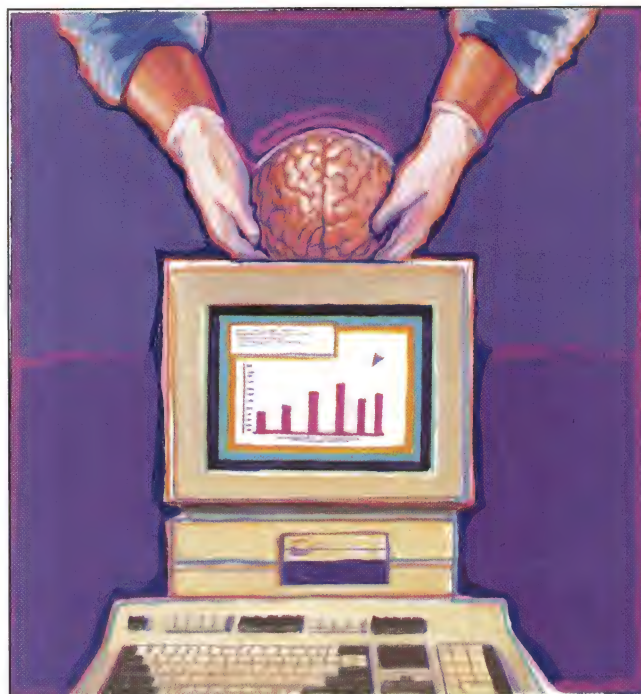
It is possible to design an extended VGA board that can display 1024- by 768-pixel resolution in interlaced mode. However, such a board couldn't display more than 16 colors. More significant, it

would be considerably slower than boards using graphics coprocessor chips.

For high-performance graphics, it makes more sense to off-load graphics functions to a specialized graphics coprocessor. Graphics coprocessor cards with resolutions beyond VGA have been available for some time. But since they have been expensive, they have generally been used only for applications demanding high resolution. Now, however, the broader demand is pushing high-resolution graphics into the PC mainstream. That, in turn, is producing a growing demand for a standard interface.

This year, two major approaches to a high-resolution graphics standard came to fruition. (For the purposes of this article, *high resolution* means anything beyond extended VGA, which is 1024 by 768 pixels.) Texas Instruments is supporting the Texas Instruments Graphics Architecture (TIGA) as a standard interface between computers using Intel microprocessors and graphics boards using its 340x0 series of graphics coprocessor chips. Western Digital, Headland Technologies, and Chips & Technologies are each pushing their

continued



versions of the 8514/A graphics adapter, which was originated by IBM for the PS/2 series.

A third possibility is a standard built around Intel's new 80860 graphics chip. However, although several companies are working on graphics boards using it, so far no one has tried to produce a standard graphics interface for the 80860.

Both would-be standards have a higher resolution than VGA. Both approach the "magic megapixel" mark (1024 by 1024

pixels, where display resolution begins to approach the limits of the human eye), and both offer many more colors and much more speed than VGA. How many more colors and how much more speed depend partly on the implementation.

Most of the time, both TIGA and the 8514/A standard are intended to be worked through software interfaces rather than going directly to the hardware. However, TIGA is completely a software interface, while the third-party

8514/A companies are making their products register-compatible with the IBM version so that programmers can go directly to the hardware if that's what they want to do.

Except for IBM's 8514/A card, no system using either standard is available yet. Western Digital announced its version of the 8514/A in early June, and TI started shipping version 1.1 of TIGA about the same time.

Both the 8514/A and TIGA have long lists of announced supporters. Over the next year, expect to be deluged with announcements for TIGA- and 8514/A-based graphics boards. Already the war of words has started between the two camps, as each side tries to influence users and software developers.

Graphics Platforms

Although TIGA provides a path to higher-resolution graphics, as is true with the 8514/A, the two quasi standards are quite different in design, intention, and implementation. IBM designed the 8514/A to be a closed hardware product and has never published the hardware specifications. TIGA is designed as an open software standard. TI is actively promoting it and is selling software development kits to help get TIGA-compatible products out into the market.

Both TIGA and the 8514/A are intended as software standards, but the third-party manufacturers of 8514/A chip sets expect that at least some software developers will want to go directly to the hardware. Thus, they are concerned about maintaining register-level compatibility with the 8514/A. TIGA was developed so that programmers would never have to go to the hardware.

The purposes behind the standards are different as well. IBM wanted a reasonably priced high-resolution graphics system for its PS/2 computers, and other manufacturers want to offer 8514/A-compatible graphics. IBM has the market power to establish a de facto standard.

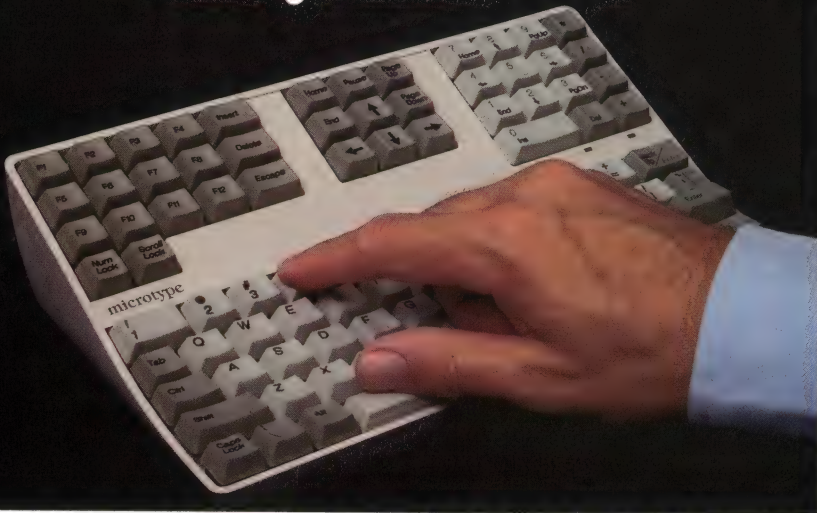
None of the manufacturers of 34010 graphics boards has that kind of market muscle. Left to their own devices, they have all offered boards with different interfaces, complicating life for software developers and programmers and burying users in different drivers.

TIGA

TIGA is an attempt to bring order to the situation by standardizing the software interface. Many companies are already offering graphics cards using TI's 34010 coprocessor. However, their interfaces

continued

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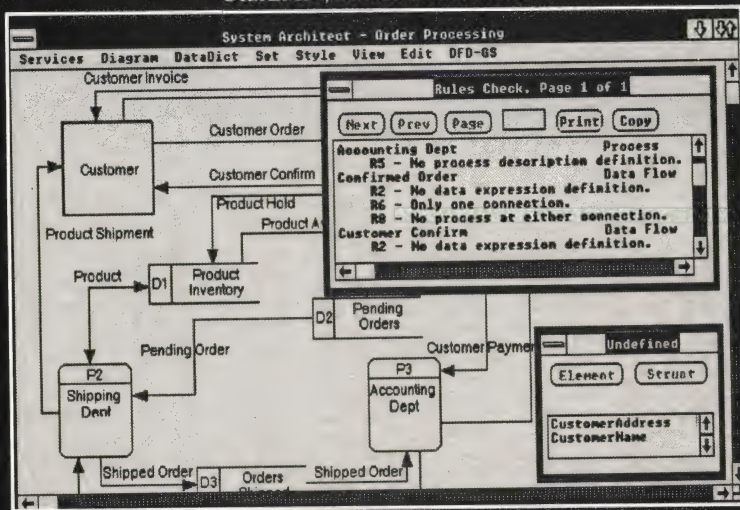
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to applications have little in common. Software companies that wanted to support the 34010 had to offer different drivers for nearly every card. In April TI took a hand and announced TIGA as a way of eliminating the differences.

TIGA is a software interface. Its purpose is to establish a standard interface between applications and system software on one hand and the 340x0-based graphics cards on the other.

The 34010 and 34020 are fast, powerful 32-bit graphics coprocessors that owe a good deal in design and philosophy to TI's 320x0 line of digital signal processing chips. Unlike the 8514/A, which takes a minimalist approach to providing additional graphics functionality, the 340x0 chips are full-blown microprocessors with a powerful set of hardware instructions for graphics operations.

The 34010 has 15 general-purpose registers, a 256-byte instruction cache, a 32-bit ALU, a barrel shifter, 32-bit internal data paths, and 16-bit I/O. Like the TI digital signal processors, the 34010 uses a Harvard architecture, with memory access and instruction execution done in parallel to increase speed. The 34020 is an advanced version that has 32-bit I/O and other added features.

In addition to its general-purpose features, the 34010 has special features for handling graphics, including programmable CRT control and a direct interface to DRAM and video RAM, or VRAM (dual-ported memory that can be read and written essentially simultaneously).

TIGA Primitives

TIGA is a full-fledged programming language with nearly 150 functions and primitives. The primitives come in three flavors: core primitives, which are always available; extended primitives, which are kept in libraries and loaded at initialization if the program needs them; and user-extended primitives, which are written by the programmer and kept in libraries like extended primitives. Functionally, there is no difference between extended and user-extended primitives, and TI says there is no difference in overhead or speed.

Generally, the core primitives are concerned with basic environment manipulation (e.g., screen clears, return foreground and background colors, and set cursor shape). Most of the drawing commands, like draw line, and the array functions, like BitBlt (a block pixel move), are extended primitives to facilitate replacing them with custom routines if the programmer desires.

Although TIGA is tied to the 340x0

family of coprocessors, it is independent of screen resolution, number of colors, and graphics constraints. Intended as a general-purpose interface, it readily adapts to new graphics equipment and new 340x0 coprocessors.

The Structure of TIGA

TIGA comes in three parts: the Application Interface (AI), the Communications Driver (CD), and the Graphics Manager (GM).

The AI consists of header files and a library that the application uses at compile and link time. It is the responsibility of the applications programmer to provide the AI, which is written using the TIGA primitives. TI sells a driver developer's kit for direct access to the standard TIGA environment and a software developer's kit for writing downloadable extensions to TIGA, including extended primitives.

The AI connects to the CD, a TSR program. This runs on the host PC and is specific to the graphics board. The CD takes function calls from the AI and passes information back and forth between the board and the host.

The CD in turn communicates with the GM on the 34010 board. Like the CD, the GM is specific to each graphics card and is supplied by the card's manufacturer. TI has a software development kit for hardware manufacturers who want to make their products TIGA-compatible. The GM includes a command executive that handles the board side of communications, the library of core primitives, and the extended and user-extended primitives downloaded at initialization.

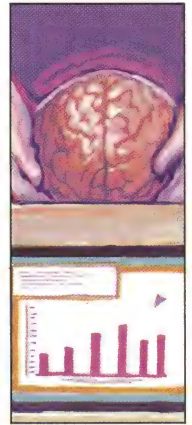
Programming with TIGA

Although graphics functions can be written directly on TIGA, the simplest approach is to write the routines as part of the program on the host and then extract them and port them to TIGA. Since the C compiler for TIGA, GSP (for graphics systems processor) C (part of the software kit from TI), is Microsoft C-compatible, this is a straightforward process.

When writing for TIGA, a programmer will probably want to exploit the inherent parallelism of a TIGA system to get more speed. This means designing the code so the graphics card can work as much as possible without referring back to the host.

To get more speed, TIGA provides two ways to pass parameters from the host computer to the graphics board. The simplest and most flexible method is to use C-packet functions. (These are not to be

Unless they are cloning an industry standard, like VGA, board manufacturers don't want to stick slavishly to a model. They want to add features that will make their products work better.



confused with the C programming language; in this case, C refers to a stack.) Parameters for C-packet functions are received on the host side and passed to the communications buffer in the graphics card's memory by the CD. From there, the parameters are pushed onto the processor's stack. The function behaves as if it were invoked local to the host.

To make this work, the GM must understand the function's arguments. In C-packet mode, each argument is a separate packet with its own header. To make writing headers easier, the TIGA.H include file contains extra defines to represent the different data types.

The general format of a C-packet function is as follows:

```
ENTRY_POINT_NAME (CMD_ID,
numpackets, packet1, ..., packetn)
```

The entry point is one of three entry points, depending on the type of function call made by the function. One entry point is for functions that do not require return data, one is for functions that do return data, and one is for functions that pass pointers to data that is modified indirectly by the function. CMD_ID identifies the function, the number of packets tells the GM the number and kind of packets, and, finally, the packets themselves arrive.

A function to fill a rectangle would be

```
#define fill rect(w, h, x, y)
cp_cmd (USER_CP (CMD_ID),
4, WORD(w), WORD(h), WORD(x),
WORD(y))
```

where cp_cmd is one of the entry points, the function's command number is stored in CMD_ID, and the function has four arguments, all WORD.

C-packet mode is simple and flexible, but it carries overhead associated with

formatting the packets and pushing the information onto the stack. The other parameter-passing mode, direct mode, avoids this overhead.

Direct mode is faster but a little more complicated to write. The raw data is simply fed into the communications buffer in GSP memory on the graphics card. The only thing placed on the stack is a parameter that is a pointer to the place where the data is stored in the communications buffer. The function must get the data from the buffer in the format it expects.

In direct mode, the length of the parameter list is expressed in 16-bit words. The entry point used determines the format that the parameters can be specified in and how these parameters will be received by the communications buffer.

For example, the most common direct-mode entry point is dm_cmd, referred to as the standard command entry point. A typical function using this entry point is the TIGA core primitive called poke_breg, which sends a 16-bit register number and a 32-bit value to be loaded into the register:

```
#define poke_breg (regno, value)
dm_cmd (POKE_BREG, 3, (short)
(regno), (long) (value));
```

The length is 3 because the parameter value is 32 bits (i.e., two words). To invoke the primitive, a parameter data_ptr would be placed on the stack to point to the location of the first parameter regno.

TI expects that most functions will use the C-packet mode. Only time-critical functions will use direct mode, and they will probably be written as C-packet functions initially and modified later. In addition to being easier to write, C-packet functions are safer. There is no

continued

Playing the Benchmark Game

If you're reading this expecting to find tables of numbers showing you conclusively which standard is the fastest, you're out of luck. There are some very good reasons for this, not the least of which is that it is physically impossible to do comparative benchmarks as this is written.

Although the 8514/A has been available from IBM for two years, none of the third-party chip makers are selling chips at this time. Western Digital announced its first chip set in early June; Headland Technology was expected to have its first chips by the fall.

Since both companies claim that their implementations will be faster than the IBM version, what is available now isn't representative of what is supposed to be the best performance for the 8514/A. Nor are TIGA boards released products. Texas Instruments has a developer's kit for its own 34010 board, but it didn't start shipping version 1.1 of TIGA until early June. No one is marketing a TIGA board for end users yet.

All this may have changed by the time you read this, but as of now, there is no way to compare the developed commercial versions of either standard. In any event, it would be difficult to come up with a fair benchmark for two such different products. Not only are the architectures, instruction sets, and design philosophies of the 34010 and the 8514/A completely different, but TIGA is explicitly a software standard

(and extensible to boot), while the 8514/A is a rigid hardware standard.

None of this has stopped Western Digital and TI from engaging in a battle of benchmarks over the merits of their approaches. On the basis of raw computing power, the 34010 probably gets the edge. It rates at about 1.2 million instructions per second compared to about 1 MIPS for the 8514/A. However, MIPS don't even begin to tell the whole story on something as specialized as a graphics coprocessor.

Western Digital claims that the IBM 8514/A is significantly faster than the 34010 and that its version will be faster yet. It has released a series of six benchmarks showing the 8514/A running much faster than the 34010. The benchmarks include line drawing and filling a polygon. In five of the six (the exception is the polygon fill), the 8514/A comes out ahead. Western Digital attributes this to the superior design of the 8514/A, especially a much better blitter.

Needless to say, TI isn't impressed. It claims that five of the six benchmarks were chosen to show the strengths of the 8514/A and ignore the chip set's major weaknesses. For example, none of the benchmarks involved drawing a curved line, since the 8514/A doesn't have a curved-line primitive.

Curved lines are immaterial, says Western Digital, since the time it takes to draw the vectors that make up the curves overshadows the time that it

takes to set up the curves.

The real test, TI claims, comes with real-world applications. TI points to its AutoCAD driver, which it claims gives superior performance over AutoCAD on the 8514/A. Western Digital's 8514/A AutoCAD driver is no faster than VGA, says TI.

Headland Technology comes back with its Windows driver, claiming it gives better performance with Windows than any other driver.

Beyond all that, TI points to its latest graphics chip, the 34020, which is about five times as powerful as the 34010 and is still TIGA-compatible. The company says that 34020 boards will run 12 to 25 times faster on redraws than the 8514/A. The 8514/A backers dismiss that as overkill, and much too expensive for the business and general markets to boot. Besides, TI says, there will be faster versions of the 8514/A in the future.

In the long run, it is probably true that the important thing for most users, at least most business users, is how well the systems perform on applications, especially when running under OS/2 or Windows. However, that will depend very strongly on the quality of the application drivers written for each standard.

In another six months or a year, it should be possible for third parties to make meaningful performance comparisons between the standards. For now, it isn't.

size checking with the fastest form of direct mode, and it is easy to overflow the buffers. Better to get everything right in C-packet mode first.

Inherent Extensibility

One of the advantages claimed for TIGA is an assured growth path. TIGA is not inherently limited in screen resolution, number of colors, or the coprocessor it uses. Already, TI has introduced the 34020, which is roughly five times as powerful as the 34010 and also TIGA-compatible.

Anyone trying to establish a standard software graphics interface has two major problems: one with software developers and one with hardware manufacturers. The problem with software companies is speed. A graphics interface has to be extremely fast or applications developers will bypass it, even at the ex-

pense of writing their own drivers for specific cards.

The problem with hardware manufacturers is market differentiation. Unless they are cloning an industry standard, like VGA, board manufacturers don't want to stick slavishly to a model. They want to add features that they think will make their products work better and faster. (Actually, even when cloning a standard, board makers like to provide extras. Most EGA and VGA cards offer features that aren't found on the IBM products.) The manufacturers want a way to add features in spite of the standard interface.

TIGA addresses the desire for extras by providing an extensible command set. Manufacturers or users with a TIGA development kit can write extensions using a compatible C compiler or assembler package and link the extensions into the

TIGA libraries. For that matter, applications programmers can write new commands and link them into TIGA.

Speed is a more difficult problem. TI has spent a lot of time optimizing the primitives and interfaces to make TIGA work as quickly as possible.

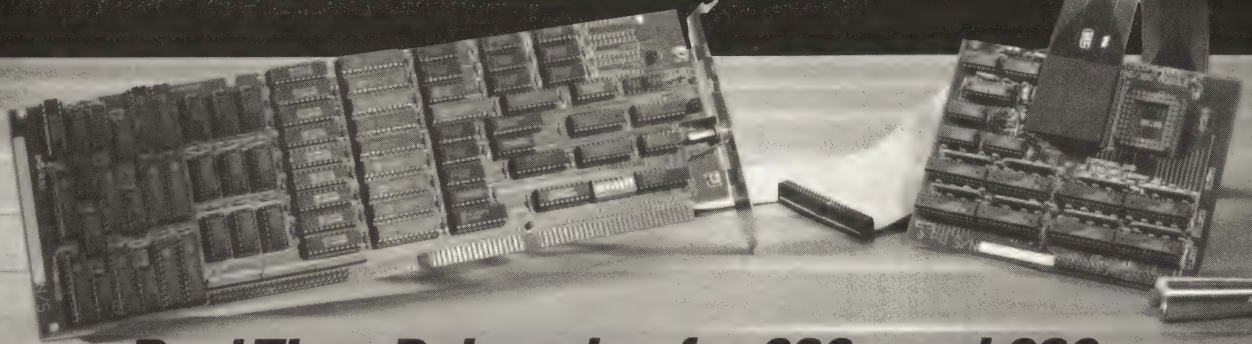
By adding extended primitives, you can optimize TIGA for particular applications. TI used a set of extended primitives to write its Windows driver, for example, and this is part of the reason why it is so fast.

Source code for the libraries is available from TI. A programmer who wants a special function to speed up a particular job can study the functions in the libraries and use the information to adapt them or to write a completely new one.

Another way to get speed with a graphics coprocessor is by exploiting the

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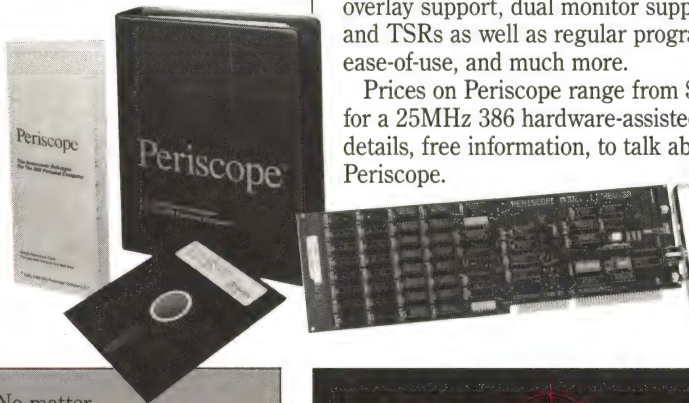


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inherent parallelism of the system. With careful programming, TIGA offers an opportunity for processing graphics commands in parallel. The CPU can start a graphics process through TIGA and work on other things until the process is finished.

The 8514/A

The third-party manufacturers' approach to cloning the 8514/A is similar to what they did with VGA, EGA, and other earlier IBM graphics standards. They are attempting to leverage off IBM's market power and at the same time standardize their hardware at the register level while providing compatible extensions to enhance their products. Already, VESA (for Video Electronics Standards Association) has a subcommittee working on an 8514/A standard.

Among IBM graphics products, the 8514/A is in a class by itself. It has not evolved from any other IBM graphics standard, as VGA was developed from EGA, nor is it backward-compatible with any of them.

In the IBM implementation, there isn't any reason for the 8514/A to be compat-

ible. The 8514/A is a PS/2 product, and the PS/2 series has VGA on the motherboard. In the PS/2s, the 8514/A adapter sits on the video bus and does nothing when VGA is active. IBM has not released a version to run on the AT bus and probably never will. The 8514/A is intended only for the PS/2 series.

Further, IBM broke tradition and did not release the hardware specification for the 8514/A. Instead, programmers are supposed to use function calls to the applications interface. This means that IBM is not committed to maintaining hardware or register compatibility in future products that use the AI.

One result is that cloning the 8514/A is harder than it was for VGA. It has taken more than two years from the announcement of the IBM product to the first register-compatible chip sets. (The 8514/A was announced in April 1987 and started shipping in July 1987.) The 8514/A involved much more reverse engineering because of less initial information.

8514/A Architecture

Physically, the 8514/A is a VLSI two-chip set consisting of a master chip (the

pixel address manager chip) and a pixel chip (the pixel data manager chip). (Chips & Technologies' implementation is all on one chip.)

The master chip contains the interface to the PC bus, the display controller, and the graphics processor. The pixel chip does the data manipulations on pixels needed to produce the images.

The display controller synchronizes signals to the display, like the horizontal and vertical sync signals. It also generates addresses for transfer cycles for the serialized portion of display memory and the interface control, if one is used. The display controller also refreshes the display memory.

The graphics processor is the most interesting part of the master chip from the programmer's standpoint. It does most of the work in creating graphics. Among other things, it generates coordinate addresses, draws lines, copies rectangles to and from anywhere in display memory, and transfers host data.

The pixel processor has a more limited job. It handles the manipulations of pixels in display memory. It can perform

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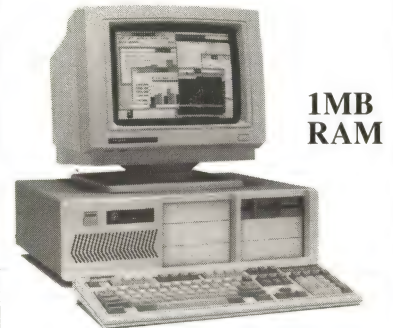
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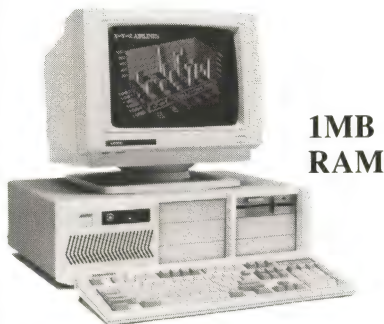
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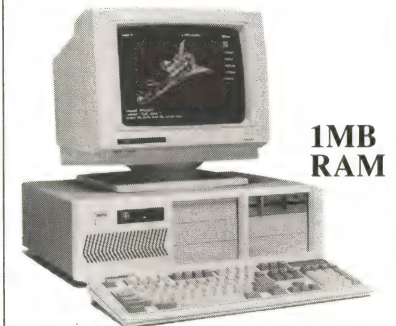
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16 logical and 16 arithmetic functions on combinations of source and destination pixels. It has two color registers for across-plane pixel processing, and eight color-compare functions to allow the selection of only certain pixels for processing. It also has read and write masks to limit processing to given display planes.

Another important feature of the pixel processor is the barrel shifter. This lets the chip do very fast alignments of source pixels during block copy operations and helps explain the 8514/A's speed on BitBlt.

In addition to the two chips, the 8514/A board includes display memory (usually 1 megabyte of VRAM), a pixel serializer chip, and a RAMDAC (for RAM D/A converter), as well as power-on self-test ROM. The pixel serializer takes the byte-at-a-time data from the display memory and converts it into a stream of bits. The RAMDAC (an INMOS IMS171 or compatible) converts the digital pixel information received from the serializer into the analog RGB signals needed by the 8514/A monitor.

Programming the 8514/A

Unlike the 340x0, the 8514/A is not a general-purpose graphics processor. It is not so much programmable as commandable (i.e., it doesn't have facilities for stored programming on the board), and its command set is both simple and not extensible.

The commands do more-complex jobs than they do with VGA. With VGA, a command essentially alters the state of the graphics system. The 8514/A does

more with a single command, but the process is more like loading commands into a queue than programming a micro-processor. One of the jobs of the PC bus interface on the master chip is to maintain the command queue, including knowing when the queue is full.

Further, IBM expects programmers to use the AI with the 8514/A. This is a function-call system using a TSR program called HDILOAD.EXE to access the graphics board.

In contrast, register programming is done through I/O ports, with each register treated as an I/O port at a specific memory location. Most of the 56 registers in the 8514/A set are word registers. The exception is the palette registers, which are all byte registers.

Each major component of the 8514/A chip set (i.e., graphics processor, display controller, and pixel processor) has its associated set of registers. For example, the pixel processor registers include the background color register, foreground color register, write mask register, read mask register, color compare register, background mix register, foreground mix register, short stroke vector transfer register, and pixel data transfer register. A number of these, like the display controller registers, are write-only.

In one sense, it is much simpler to program the 8514/A than to program a TIGA board. You use the appropriate function calls (under the AI) or place the appropriate values in the registers. In either case, the command set is sparse compared to that of TIGA. There is less to remember and deal with.

But writing useful programs with the 8514/A isn't necessarily simple. Even with the AI, the programmer has to deal with the 8514/A on a very basic level. Because the functions are limited, the programmer may have to spend more time figuring out how to make something happen. One 8514/A proponent compares programming the card to programming a plotter.

For example, to perform a BitBlt, the program first executes a command telling the 8514/A what kind of transfer is required (e.g., host to display or display to host). A second command gives the address to be read from or written to.

Third-Party Enhancements

Both Western Digital and Headland Technology have announced their own 8514/A chip sets, which are compatible right down to the register level. Like the many third-party VGA boards, these chip sets are designed to go beyond IBM by offering more features and better performance.

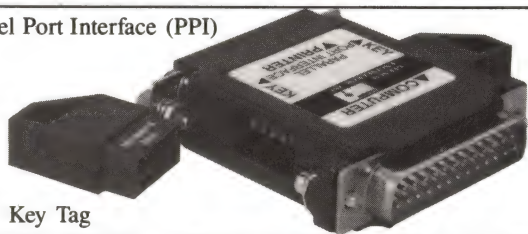
Western Digital calls its chip set the Personal Workstation Graphics Array 1. It includes a number of features not found on the 8514/A, including the ability to support interlaced and noninterlaced monitors with a maximum resolution of 1280 by 1024 pixels. The clock speed of the chip set is 60 MHz, 30 percent faster than the IBM version, so it speeds up operations like BitBlt and rectangle fill. The PWGA1 also has a shorter memory-transfer time, which further speeds up operations.

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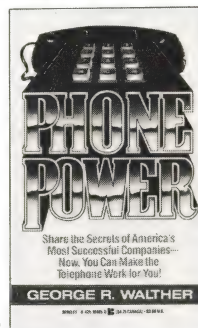
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In addition, the PWGA1 features a turbo BitBlt mode that can double the speed on 16-color images. In this mode, 8-bit data transfers from the on-board VRAM are treated as two 4-bit transfers, meaning that two pixels can be read per transfer. Four bits are sufficient to define 16 colors, and 8 bits can define 256 colors. If the application is using 16 or fewer colors, the PWGA1 can combine two 4-bit transfers into one 8-bit transfer, cutting the time needed in half.

Going to the Hardware

The conventional wisdom of MS-DOS graphics has always been that programmers will want to go to the hardware to get the maximum speed on their displays. Working through a software interface is significantly slower. Most manufacturers think this will be less of an issue with the 8514/A.

There are some significant differences between the 8514/A and the previous standards. For one thing, the 8514/A is a good deal faster, even through the AI. For many applications, it has enough speed that developers won't feel the need to bypass the software interface.

A second difference is that the 8514/A is designed to work in the brave new world of OS/2. The IBM version is available only on PS/2s, which are intended to be IBM's platforms for OS/2. It is harder to play games with the hardware under OS/2 than it is under MS-DOS.

This combination of speed and difficulty means that most applications software developers won't be tempted to go directly to the hardware. However, system software developers may very well want to write to the registers to get as much speed for their applications as they can. This is the approach that Microsoft took in developing its 8514/A drivers for Windows.

Interlaced Video

Another peculiarity of IBM's 8514/A is that it produces an interlaced display. Headland Technology and Western Digital say their chip sets can do the full 1024-by-768-pixel display without interlacing.

Interlaced modes are hardly new. Broadcast TV uses an interlaced system. So, in fact, does the Commodore Amiga. However, they have been uncommon in MS-DOS systems until now.

The advantage of an interlaced mode is that it lets you double the vertical resolution of a system without having to double the scan frequency of the monitor. Since the cost of a monitor increases with the scan frequency (although not lineally), that holds down costs.

In the case of the 8514/A, that could have been a significant cost. Even before the standard was announced, a number of multisync monitors were available that almost reached the 8514/A's frequency of 33 kHz. Providing 8514/A resolution without interlace would have meant going to a 60-kHz monitor, well outside the PC state of the art at the time the system was announced.

In designing the 8514/A, IBM was clearly concerned about keeping down the scan rate of its monitor. The logical display resolution would be 1024 by 960 pixels. Backing off the horizontal scan rate to 768 pixels cut the frequency requirements.

A lower vertical resolution also makes it easier to avoid flicker, one of the inherent disadvantages of interlaced video. In effect, interlacing cuts the screen refresh rate in half, since it takes two scans to completely refresh the screen. If the effective refresh rate is too low, the results are very noticeable.

The typical scan rate on a computer monitor is 60 times per second. This is

fast enough that no flicker is noticeable. Doubling the vertical resolution and halving the refresh rate would drop the scan rate to 30 times per second, slow enough that flicker becomes apparent.

By holding the vertical resolution to 768 pixels, IBM was able to use a scan rate of 44 times per second. This is fast enough to significantly reduce flicker. In addition, the 8514 monitor uses a long-persistence phosphor, and the combination gives adequate display quality for almost any application.

Is Adequacy Sufficient?

The 8514/A appears to be designed with the philosophy that adequacy is sufficient. It is not a full-fledged graphics coprocessor with an extensive library of built-in functions. Instead, it is a rather simple processor with limited, hard-wired instructions.

In theory, the more powerful the graphics coprocessor, the better. This is the philosophy behind the 34010, the 80860, and most other graphics coprocessors. In practice, a powerful coprocessor trades off cost and ease of programming to get power. IBM apparently decided it made more sense to settle for less power in a less-expensive product.

As a result, the 8514/A's instruction set is limited. Programming it is easy in the sense that once you decide how to do something, doing it is very straightforward. But figuring out how to go from a requirement to a programming strategy may take some thinking.

Notably missing from the 8514/A's instruction set are arc-drawing primitives. Nor is there a polygon-fill primitive, although polygon fills can be done readily using the Begin Filled Area and End Filled Area commands.

Although the command set is fixed in

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Logitech products: 1212151, 12 x 17.

Summagraphics products: Scanman PC, Scanman PS/2.

Hewlett Packard products: HP740A, HP7475A, HP750, HP750 L, HP7576 EXL, HP SCANJET.

Houston Instrument products: HI DMP-52, HI DMP-52MP, HI DMP-56A, HI DMP-51, HI DMP-62, Image Maker.

Printers: Epson (LX810, LQ850, FX850, FX1050), NEC (P2200, P5200), Diconix, Kodak (150P/300), Toshiba (321SL, 341SL, 351SX), Brother (M-172AL, HR20), Okidata (ML 182 Turbo, ML 172, ML 380, LASERLINE 6, ML320).

Panasonic Laser Printers: BROTHER HL-8e, H-P LaserJet Model 2 / IID, H-P Deskjet, NEC LC890, PCLIP DATA 25 in 1 Cartridge, TOSHIBA Page Laser 12.

Drives, Tapes & Cards: FLOPPIES, DRIVES & TAPES. Includes CONNER, GENOA, IOMEGA, IRWIN, MOUNTAIN, MICROPOLIS, MOUNTAIN 4440, MOUNTAIN 150M, PLUS, PLUS 20, PLUS PS/2, PLUS PS/2 MC System Kit, PLUS DEVELOPMENT 40 Meg, PRIAM, SYLGEN, SYLTEC.

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Novell Network Interface Cards: ARCNET PC110 LANboard PS/2, ARCNET PC130 LANboard, ARCNET PCI 30e LANboard, ARCNET SMC 16-Bit File Server Board, ARCNET SMC 16-Bit Workstation Board, ETHERNET Interface Connector (NE1000), ETHERNET Plus Board (for 286) (NP600), G-NET Interface Card w/Cable, NOVELL NE2000, THOMAS CONRAD 16 Port Hub, THOMAS CONRAD 8 Port Hub, Ethernet Terminators.

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Modems & Communications: EVEREX 1200B / 2400B, EVEREX 2400 Ext. / 2400 PS/2, INTEL 2400 Internal, INTEL 2400 External.

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FAX Machines and Boards: Complete Fax 9600, Quadram J/Fax 9600, Quadram J/Fax Port.

Software: WORDPERFECT 5.0 5.25"/3.5", ASHTON TATE dBase III+ / dBase IV, ASHTON TATE Multimate Advantage II, LOTUS 1-2-3 5.25"/3.5" V2.2, LOTUS 1-2-3 V3 / LOTUS Networker, BORLAND Paradox 3.0, BORLAND Quattro / Sidekick, MICROSOFT Excel / Windows 386, MERIDIAN Carbon Copy, SYMANTEC Q&A, SOFTWARE PUB. Harvard Graphics, XEROX Ventura Software Version 2.0.

Mono Monitors & Cards: CDW™ Color / Mono Cards w/P, HERCULES™ Color / Mono Cards w/P, AT&T Monochrome Monitor, AMDEK 410A / 1280, COMPAQ Mono / VGA Mono, IBM PS/2 8503, SAMSUNG Amber, PG5 MAX 12E / MAX 15, PACKARD BELL Green or Amber.

Color Graphic Monitors: IBM PS/2 8512, IBM PS/2 8513, SAMSUNG RGB Color, MAGNAVOX 8762.

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Mice: LOGITECH C9 Serial / PS/2, LOGITECH Bus, MICROSOFT Mouse (Bus Version), MICROSOFT Mouse (Serial Version), MICROSOFT Mouse w/Windows, MOUSE SYSTEMS (Serial Version), MOUSE SYSTEMS (Bus Version).

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hardware, the chip set has considerable potential for expansion in resolution and color. For one thing, according to Headland Technology, the chips themselves will support resolutions of 1280 by 1024 pixels, even if the present boards won't. That means that increasing the resolution will be fairly straightforward.

Equally significant, one address chip can handle up to four pixel chips. That would let the 8514/A do 32-bit color at the same speed as the present 8-bit color.

IBM Moves

The 8514/A not only breaks new technical ground for IBM-compatible graphics standards, it also poses a marketing risk that earlier IBM-compatible standards did not. Because IBM did not release any of the hardware specifications, there is nothing to stop the company from coming out with a completely new product tomorrow that conforms to the software specification.

On the other hand, IBM has said that it

intends to put the 8514/A on the motherboard of future models of PS/2s. It has indicated that it intends to stay with the 8514/A for several years, albeit with expansions and extensions.

Further, the 8514/A's backers say that they expect to build enough momentum in the market that it will be a standard no matter what IBM does. If there are 2 or 3 million 8514/A systems in users' hands, applications developers are going to provide drivers for the 8514/A.

Upgrading to the 8514/A poses a dilemma for users. It is not backward-compatible, and not all software comes with 8514/A drivers.

There are several ways around this. One of them is to install the 8514/A adapter alongside a VGA card and use the standard pass-through connector that is part of the VGA specification. That works, but it takes up a second expansion slot. In addition, in some VGA implementations, you run into a memory conflict. Third-party VGA board manufacturers have added features and modes to the boards, so their BIOSes are larger than IBM's, and their implementations run over into 8514/A memory space.

Another possibility would be for manufacturers to offer boards that have both VGA and 8514/A on them. That would be more expensive than a regular 8514/A card, but it may prove popular with users with existing systems.

A Standard for the 1990s?

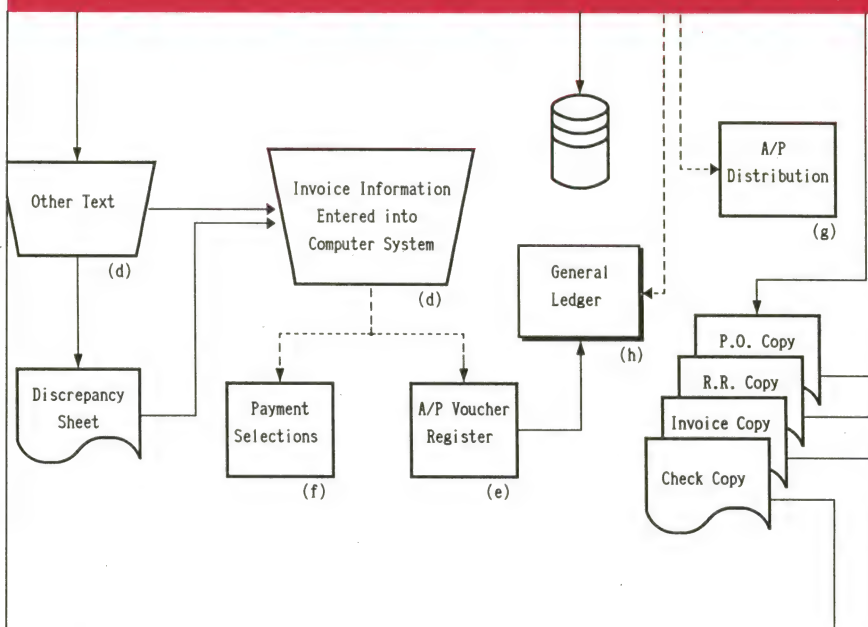
As this is written, it is much too early to tell which graphics system will become the next standard. Both the 8514/A and TIGA are attractive, and they both have strong and weak points.

TIGA offers a uniform, resolution-independent software interface that can be extended to meet programmers' needs and can grow to handle new generations of graphics coprocessors. The 8514/A follows the classic path of turning an IBM product into a standard. It includes the ability to access the hardware directly for maximum speed, and the hardware may very well be less expensive than TIGA. Its backers also claim that it is faster than TIGA.

Technically, both of these proposed standards represent a significant advance over VGA. Which of them is successful will probably depend at least as much on the market factors as on their inherent benefits. ■

Rick Cook is a freelance writer in Phoenix, Arizona, specializing in computers and high-technology subjects. He can be reached on BIX as "rcook."

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IS IT REALLY SUPER?

The Super VGA standard is both a beginning to solving some problems and an end to simple solutions for others

Bill Nicholls

CGA, Hercules, EGA, PGA, VGA, 8514/A—haven't we had enough? With resolutions ranging from 320 by 200 pixels to 1024 by 768 pixels and color options from monochrome to 256 colors from a palette of 256,000, we seem to have overdone the graphical user options a bit. What started as a simple choice between monochrome and color has become a confusing and expensive set of options for users and has escalated into a nightmare for manufacturers and programmers of video display adapters.

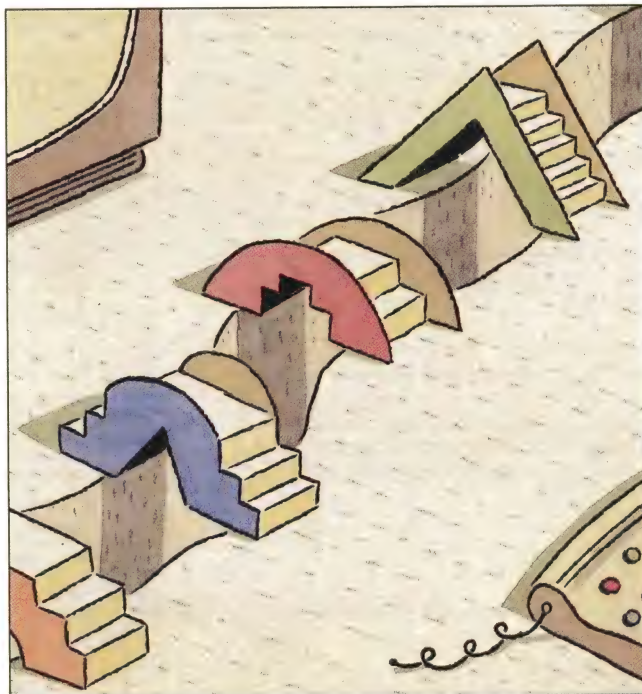
Each of these classes of display adapters has one or more standard text modes, ranging from 40 columns by 25 rows to 80 columns by 50 rows, and standard graphics modes that range from 640 by 200 pixels by 2 colors (CGA) to 640 by 480 pixels by 16 colors (VGA). Most of the modes in the earlier adapters are supported in the later ones, though sometimes with different setup parameters. For true IBM modes, all compatible adapters support the setup via BIOS calls.

In addition, almost every maker of display adapters has added special text and graph-

ics modes (via hardware and BIOS extensions) that differentiate its product from others. For text, these special modes range up to 132 by 60 characters. For graphics, they range up to 1024 by 768 pixels, interlaced and noninterlaced, as well as 800 by 600 pixels in 16- and 256-color options.

As a result, software companies that produce graphics software have provided

limited support for the special extended modes unique to a specific adapter. Thus, the video-adaptor manufacturers have had to greatly expand their programming and technical-support effort to provide software drivers for each graphics package in order to solve your installation problems. And you still have to figure out what combination of modes and software gives you the best result with your current display!



How Bad Can It Get?

Five chip sets currently support VGA-compatible displays: Renaissance, ATI Technologies, Western Digital Imaging (Paradise), Video Seven, and Tseng Labs. All have extensions requiring different programming to activate similar modes. A similar number of chip sets exists for the EGA standard and extensions, and the 8514/A has both a software application interface and a decoded hardware interface from Western Digital. 8514/A clones are expected soon and could further expand the incompatible setup and programming problem. You could have 30 to 60 independent sets of code for each application to drive the most common video adapters

continued

in the most common graphics modes.

With the exceptions of Microsoft Windows and GEM for DOS, Presentation Manager for OS/2, and X Window for Unix, no common driver interface exists for graphics applications. Graphics applications now face a two-level software-support decision: which interface standards they should support, and which stand-alone adapters DOS should support. To support the growing number of environments and video adapters, each graphics application must devote more programming resources to the graphics interface rather than to the application.

The good news is that a group of video chip, board, and display vendors saw this problem coming and formed an independent organization—VESA, the Video Electronics Standards Association. This organization recommends standard BIOS and programming interfaces for the extended graphics modes that hide the incompatible hardware implementations.

The bad news is that the task is complex and must be done in a backward-compatible manner so as not to orphan the current installed base of VGA cards. The VESA VGA BIOS extension proposal version 2.0, called Super VGA, was issued in April. It will take time for final agreement and implementation of the new standards, and still more time to rewrite or upgrade the software drivers.

The Standards

The term *Super VGA* refers to video graphics products that implement a superset of the standard IBM display

adapter. The VESA Super VGA Standard is the proposed software interface that will isolate the hardware differences and provide information in a hardware-independent manner. This means you will finally be able to write graphics software without needing special code for each specific chip set or having to identify which adapter you're using.

VESA is proposing standards for determining the video environment, programming support, compatibility, mode numbers, and BIOS functions. The video-mode numbers are 15 bits wide, while current VGA video-mode numbers are 7 bits wide and range from 00 hexadecimal to 13h. Manufacturers have established extended modes in the range from 14h to 7Fh. Values in the range 80h to FFh are not allowed since bit 7 is a Clear Video Memory flag. Except for

mode 6Ah, all other VESA modes will equal or exceed 100h (see table 1).

An extended BIOS support using extended function 4Fh in the video interrupt 10 handler is also proposed. Function calls will return status in the AX register concerning support or nonsupport, success or failure (see table 2).

In addition to these functions, further analysis and discussions are aimed at other aspects of the video adapters. These include the following:

- Extended video-memory mapping, which could simplify windowing software by insulating it from most of the hardware details.
- External palette control to 6- and 8-bit D/A converters, which could create a uniform interface to either a 256,000-color palette or a 16-million-color palette.
- Variable start address for the CRT, important in animation techniques.
- Standard timing parameters for the display so that monitor manufacturers can provide monitors that synchronize without adjustment and provide the proper picture size at any resolution.

Table 1: *The VESA video-mode numbers are 15 bits wide, while current VGA video-mode numbers are 7 bits wide. Except for mode 6Ah, all other VESA modes will equal or exceed 100h.*

PROPOSED VESA MODES		
Mode Number	Resolution	Number of colors
6Ah	800 × 600	16
100h	640 × 480	256
101h	800 × 600	256

Table 2: *VESA function calls will return status in the AX register concerning support or nonsupport, success or failure.*

PROPOSED VESA FUNCTIONS

Function number	Purpose
00h	Return Super VGA information. This function returns a pointer to a buffer containing supported Super VGA capabilities and other pointers.
01h	Return Super VGA mode information. This function returns a pointer to a detailed table of size, attributes, and resolution for a specific Super VGA mode.
02h	Set Super VGA video mode. This function sets the desired mode, if available; otherwise, it leaves the environment unchanged.
03h	Return current video mode.
04h	Save or restore Super VGA video state.
05h	Set CPU video-memory window. This function allows direct access to the hardware-paging registers of the video memory.

How Does This Affect the End User?

Except for the installation difficulties, as an end user, you don't see most of the current problems directly. What you *do* see are long delays required for the extended graphics modes, and separate drivers for each graphics software package for each specific adapter family.

VESA has yet to make an impact on the end user, but once the standards are accepted, you will see fewer but more-functional software drivers. In addition, switching to a new video display adapter usually won't mean getting a whole new set of drivers, since a driver written to the VESA standard should work with any VESA-compliant adapter.

Performance Issues

VESA standards may solve the incompatibility problem, but higher resolution presents another problem. Higher resolution means more pixels; more pixels mean more operations to update each screen; and more operations mean a slower response to any change.

Given today's systems and adapters, a 4.77-MHz computer will be slow at supporting EGA graphics. For basic 8-MHz ATs, VGA at 640 by 480 pixels is probably the best resolution with acceptable graphics performance. A 12-MHz AT can support VGA at 800 by 600 pixels, but 1024 by 768 pixels needs a 16-MHz

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Table 3: Most graphics software runs at 640 by 480 pixels today, so the processor is handling 2.4 times as many pixels as CGA. The higher-resolution screens will clearly be slower.

EFFECT OF RESOLUTION ON NUMBER OF PIXELS

Video mode	Resolution	Number of pixels	Percent of CGA
CGA	640 × 200	128,000	100
EGA	640 × 350	224,000	175
VGA	640 × 480	307,200	240
Super VGA	800 × 600	480,000	375
8514/A	1024 × 768	786,432	614

AT or 80386-based machine for good performance in graphics modes.

However, not all the limitations are in the processor—a 16-bit VGA will be faster than an 8-bit VGA, provided the hardware and software used can handle 16-bit graphics access. Unfortunately, this is the exception rather than the rule.

Look at this another way. Since most graphics software runs at 640 by 480 pixels today, the processor is handling 2.4 times as many pixels as CGA, but the

higher-resolution screens will clearly be slower (see table 3). Two other factors also affect the delays: access to the video adapter memory, and the number of operations required to change a single pixel.

EGA is particularly bad for memory access, as five out of six memory accesses must be dedicated to refreshing the display, leaving only one out of six for updates. This is the primary reason for slow EGA displays.

VGA has a different problem. While

memory access is faster, the larger pixel array requires as many as five I/O commands for each update due to the segmented addressing required to access 256K bytes or 512K bytes from a 64K-byte address space. While in 16-color mode, VGA can update two pixels at once; but in 256-color mode, it must access each pixel separately.

Adding insult to injury, many VGA adapters still have 8-bit registers even if they have 16-bit interfaces to the AT bus. Add further delays due to slower ROM BIOS access, and the situation can't get much worse. The amazing thing is that good performance is delivered in most cases because of skillful programming in the graphics drivers, which are finely tuned to specific adapter hardware.

To accomplish further performance gains in the high-resolution area (800 by 600 pixels and up), hardware assistance in the form of dedicated graphics processors will provide the repetitive pixel manipulations currently dependent on the host CPU. Graphics chips available today include the Intel 82786, the Texas Instruments 34010 and 34020, and,

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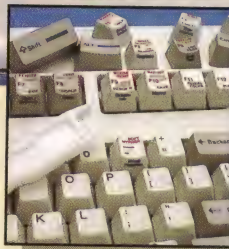
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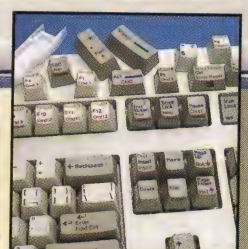
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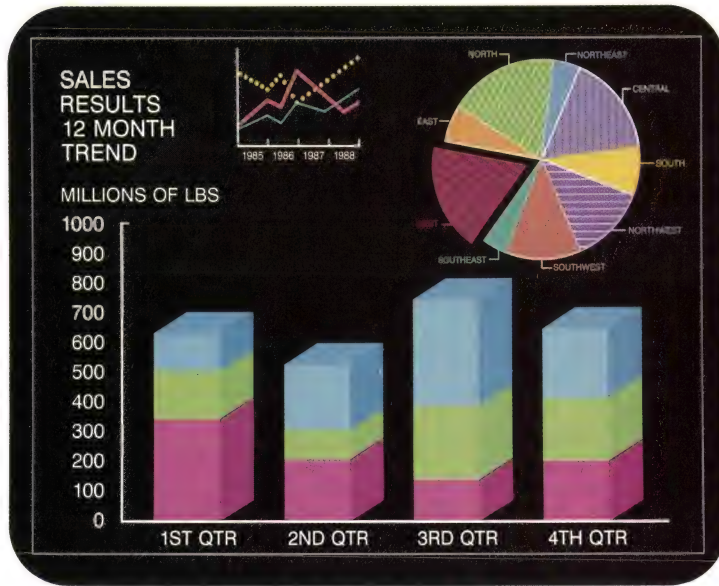
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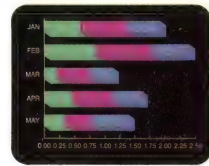
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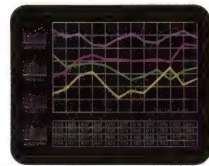
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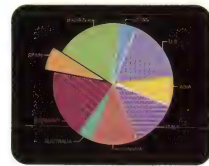
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expected near the end of this year, the chip supporting the IBM 8514/A.

However, this is only half the equation. Graphics code today is written for host-processor bit- and pixel-twiddling. Changing to outboard chips will require at least a rewrite of the graphics driver, and maybe a redesign of the interface. Functions with repetitive operations, such as line drawing and area fill, are quick to pass as parameters, but complex shapes may be slower than the host CPU can handle. These complex operations will require bit maps of graphics objects to move rapidly between the host CPU and display processor.

Future Directions

Except for Texas Instruments' TIGA standard for 340x0 boards, the issue of standards for "smart" video adapters is two years behind that of the VESA standard for VGA boards. As these boards drop below \$1000 in the 1990s and become mainstream components, the problem of proliferation of interfaces will recur unless VESA or a follow-on group soon begins the lengthy process of achieving a standard through consensus.

In addition to the current proposed VESA standard, other standards work is planned, and new working groups include the 8514/A interface. To those groups should be added a group for analysis of performance issues, another for operating environments like Windows, and a third to study the transition issues as software has to support the smart graphics adapters.

As an end user, you can look forward to Super VGA as both a beginning and an end. Graphics-driver standards are beginning to solve the problems of incompatible hardware, but simple CPU support for higher-resolution displays is coming to an end.

For the near future, 1024 by 768 pixels will be an economic limit for most of us for graphics displays. This is also the approximate limit for reasonable performance when driven directly by an 80386-based CPU. For the next 8 to 12 months, these displays will become more cost-effective and popular as software support catches up with hardware capability and production volume enables prices to come down. Beyond that, future advances of graphics resolution and performance will depend largely on beginning to create new standards now. ■

Bill Nicholls has a B.S. degree in physics from Notre Dame University and is the owner of BGW Systems (Puyallup, WA). He can be reached on BIX as "billn."

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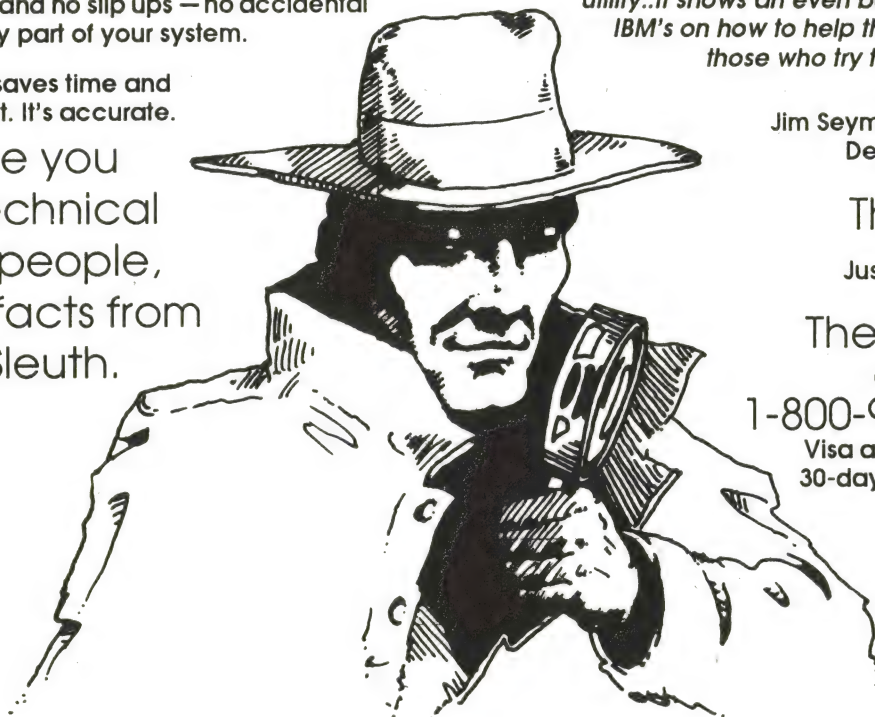
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Recently, Dr. Pournelle looked at Northgate's 80386 Pipeline Page Mode system and reported in BYTE July, 1989 (excerpted):

*Jerry Pournelle holds a doctorate in psychology and is a writer who also earns a comfortable living writing about computers present and future.



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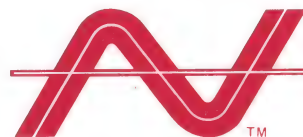
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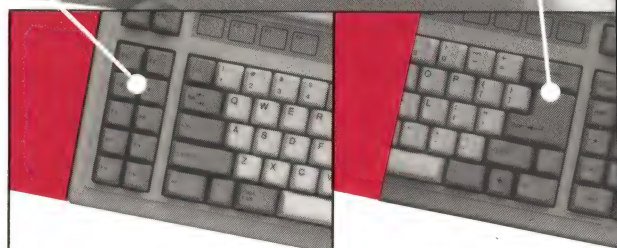
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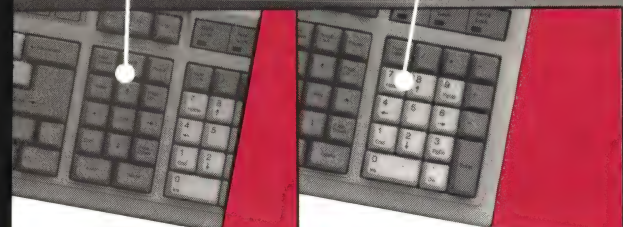
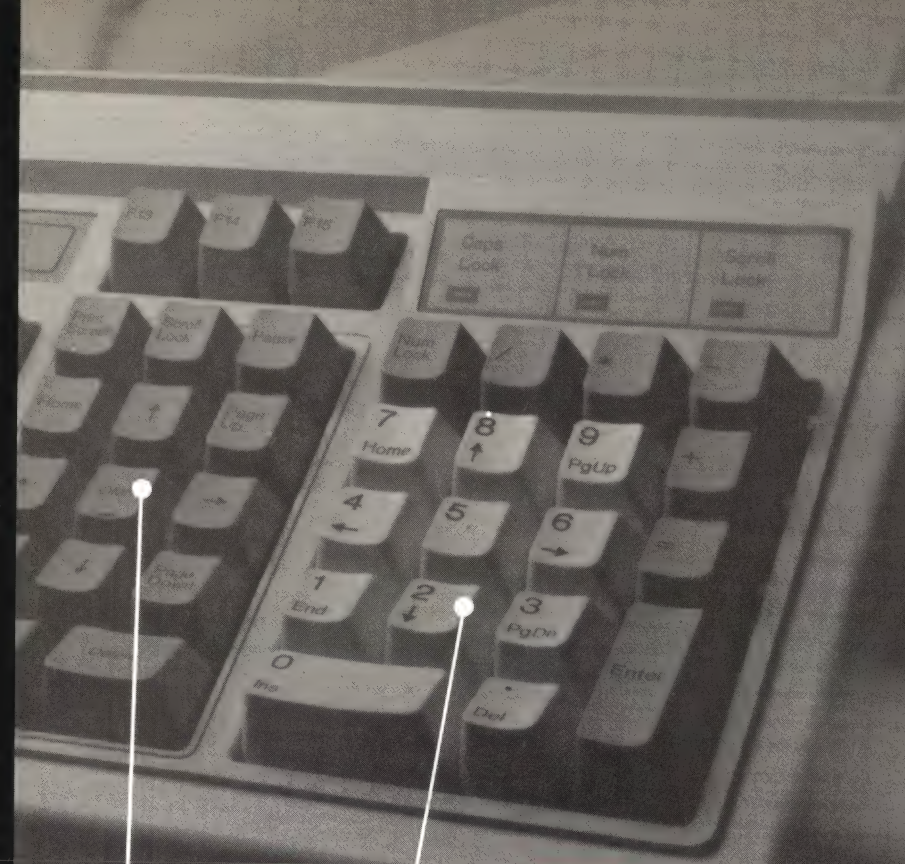
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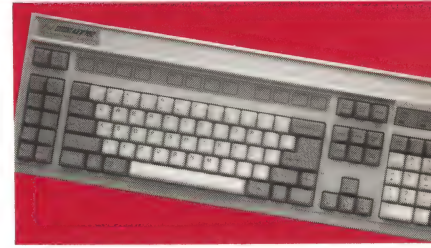
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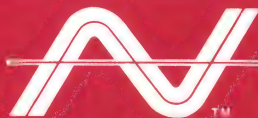
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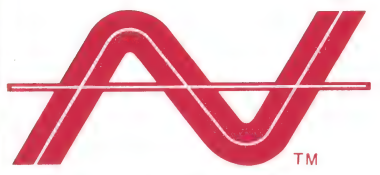
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Please complete all appropriate sections, providing at least two year's residence and employment history. This will enable your application to be processed as quickly as possible. If you are self-employed, please be sure to complete section "d" on back.

Applicants must be 18 years of age or older.

a. Your Personal Information Requested Line of Credit \$ _____

Your Name: First _____ Initial _____ Last _____ Date of Birth: Mo. _____ Day _____ Yr. _____ Social Security Number: _____

Present Address: Street _____ Apt. # _____ City _____ State _____ Zip _____ Home Phone: () _____

Date of Residence: Month _____ Year _____ Monthly Payment: \$ _____ Buy _____ Rent _____ Other _____

Previous Address: _____ Dates of Residence: From _____ To _____

Your Employer: (If self-employed, see rear panel.) Date of Employment: Mo. _____ Yr. _____ Position: _____ Monthly Income: Gross \$ _____ Net \$ _____

Employer's Address: Street _____ City _____ State _____ Business Phone: () _____

Previous Employer: _____ Address: _____ Dates of Employment: From _____ To _____

Income from alimony, child support or separate maintenance payments need not be disclosed if you do not wish to have it considered as a basis for repaying this obligation. I have received since: (Date) _____ Monthly Income: Gross \$ _____ Net \$ _____

Name and Address of Nearest Relative Not Living With You: _____ Relationship _____

b. Credit Information Include joint applicant's information, if joint account requested.

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Bank Account: _____ Checking Savings

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Joint Applicant's Name: First _____ Initial _____ Last _____ Date of Birth: Mo. _____ Day _____ Yr. _____ Social Security Number: _____

Address: Street _____ Apt. # _____ City _____ State _____ Zip _____ Date of Residence: Mo. _____ Yr. _____ Home Phone: () _____

Employer: _____ Date of Employment: Mo. _____ Yr. _____ Position: _____ Monthly Income: Gross \$ _____ Net \$ _____

Employer's Address: Street _____ City _____ State _____ Business Phone: () _____

d. Self-Employed Information Complete this section only if you are self employed.

Business Name: _____ Proprietorship Corporation Partnership

Business Address: _____ Business Telephone: () _____

Description of Business: _____ Your Position: _____ In Business Since: _____

Your annual income from business: _____ Business' annual income: (gross) _____ (net) _____

You must provide at least one of the following:

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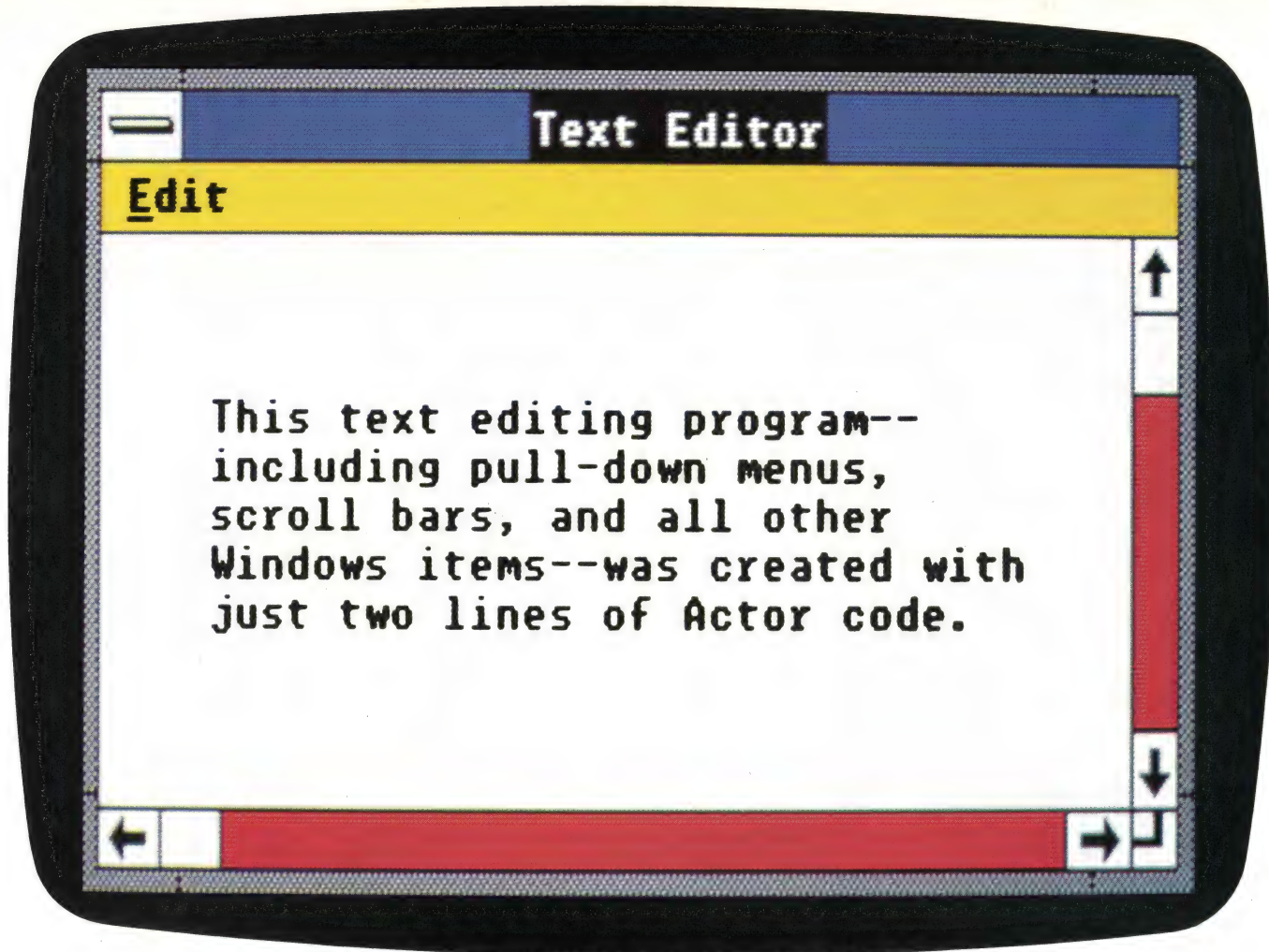
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SQL: A DATABASE LANGUAGE SEQUEL TO dBASE

A look at SQL's command structure shows why it's likely to become a new standard

Mark L. Van Name and Bill Catchings



For many years, dBASE has been the dominant microcomputer database language. While dBASE undoubtedly still has a long life ahead of it, another database language, SQL (pronounced "sequel"), is emerging as a second standard for both database servers and stand-alone microcomputer databases.

SQL has for several years been the standard language for mainframe and minicomputer relational database systems. As such, it offers microcomputer users a single language for both stand-alone and host databases. SQL is particularly good for working with such host or server databases, in large part because it can manipulate groups of records at a time—an important capability when you're reading records over a network.

SQL also tries to minimize the effort that a database programmer must expend to retrieve data. It is a *nonprocedural* language: You tell a SQL database system what data you need, not how to get that data.

SQL is not, however, a full application development language like dBASE. While many SQL vendors have added programming extensions to the language, it's designed to work in conjunction with such traditional programming languages as COBOL, Pascal, PL/I, or C.

A Long History

SQL has been around since 1974–1975, when IBM developed the first version, SEQUEL (for Structured English Query Language), at the company's San Jose research center as part of a prototype relational database system, SEQUEL-XRM. A second version, SEQUEL/2, followed in 1976–1977 as part of IBM's System R relational database prototype.

SQL emerged from the research world in 1979 in a commercial database system, Oracle, from Oracle Corp. (then Relational Software). Oracle actually beat IBM to market with SQL, but IBM brought out its own products in the early 1980s—first SQL/DS for DOS/VSE mainframes, and then DB2 for MVS systems.

Where IBM goes, others are sure to follow; today, over 100 vendors offer versions of SQL. SQL microcomputer implementations abound, including IBM's OS/2 Extended Edition Database Manager, Oracle Corp.'s Oracle, Relational Technology's INGRES, the Sybase/Microsoft/Ashton-Tate SQL Server, the SQL component of dBASE IV, and Gupta Technologies' SQLBase.

All these versions follow, to at least some degree, a SQL standard that the X3H2 Database Committee of ANSI started developing in 1982. That group's initial proposal, which ANSI ratified in 1986, was very similar to IBM's DB2 dialect of SQL.

SQL's Many Faces

The ANSI SQL standard establishes a common target for the many SQL vendors, but it by no means precisely defines a single, all-inclusive language. In fact, no two versions of SQL, even those that are ANSI-compatible, are identical. The differences between SQL versions are due largely to the two different ways in which users and programmers must work with SQL.

Most SQL database vendors offer one or more interactive utilities that accept SQL. With such tools a user can, for example, write a SQL statement that requests the records of all the salespeople in Minneapolis, and then see those records. The dialects of such interactive products generally follow the ANSI standard, but they cannot do so completely.

That inability isn't the fault of the vendors; the ANSI standard doesn't define an interactive version of SQL. Instead, it concentrates on making SQL work with such traditional programming languages as COBOL and PL/I. The standard actually defines two different ways for SQL to work in programming languages.

Differences between interactive and programming language versions of SQL are almost unavoidable because of the way the two environments must handle multiple records that satisfy a single request. An interactive environment can just display

continued

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those records in a suitable format, hiding any programming details from the user. But a programmer must contend with a limitation of most traditional languages: They are not designed for procedures that return a variable number of records, as SQL statements can.

In the following discussion of SQL statements, we'll use a syntax much like what you would find in an interactive SQL utility. Then we'll explain how the ANSI standard lets you use SQL statements in a programming language. Because SQL is a large and comprehensive language, and one whose complete explanation has filled many books, we will necessarily cover only its key parts. They should serve, however, to illustrate how SQL works and what you can do with it.

Data by Definition

SQL is in a sense two languages in one: It's a data definition language (DDL), with which you can define a database, and it's also a data manipulation language (DML), with which you can manipulate the records in that database. We'll start with the DDL.

SQL is based on the relational database model, where a database is a collection of one or more named tables. Each table is an unordered collection of rows, each of which has a fixed number of columns. Each column has a heading (name) and a data type. ANSI SQL defines three basic data types: character strings, exact numbers, and approximate numbers—roughly the strings, integers, and floating-point numbers of most programming languages.

Obviously, these tables, rows, and columns have analogs in traditional files, records, and fields. But they differ in that SQL lacks an order for the rows in a table. If you ask for all the rows that satisfy some criteria, SQL will return those rows to you in an implementation-specific order—and it won't necessarily maintain that ordering in subsequent queries. If you want to get the rows back in a specific order, there's a SQL verb that lets you do so.

Unlike the rows, the columns in a table do maintain the order in which you define them. That order is important primarily to the INSERT command, which we'll discuss later.

In addition to permitting you to define individual tables, any relational system must enable you to relate those tables. When you want to express a relationship between rows in two tables, you use values in columns. Consider the following two simplified tables:

Table Name: Employees
Columns: Employee_Id, Last_Name,
First_Name, Address, City,
State, Zip

Table Name: Dependents
Columns: Employee_Id, Last_Name,
First_Name

To make "Donald Smith" a dependent of "Judith Smith," you put Judith Smith's employee ID in the Employee_Id column of Donald Smith's dependent row. The two columns that form the relationship—in this case, the Employee_Id column in each table—must have the same data type.

While you use this mechanism to relate rows, in SQL you never define such relationships. Instead, you define the tables and columns and then use the relationship in record retrievals when you need it.

SQL translates the relational database model into a database definition with several DDL statements. A SQL database definition is a group consisting of one or more schemata. A *schema*

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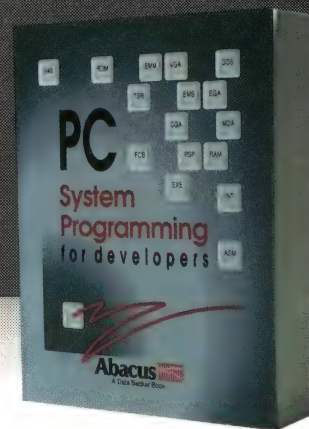
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is a definition of the part of the database that each user owns. For example, the SQL statement

```
CREATE SCHEMA AUTHORIZATION USER1
```

creates a schema that USER1 owns.

Once you've created a schema, you can define its tables, all of which start out empty. To define the two sample tables from above, you would issue the following commands:

```
CREATE TABLE Employees
( Employee_Id DECIMAL(5) NOT NULL UNIQUE,
  Last_Name CHAR(15),
  First_Name CHAR(15),
  Address CHAR(15),
  City CHAR(15),
  State CHAR(2),
  Zip CHAR(10) )
```

```
CREATE TABLE Dependents
( Employee_Id DECIMAL(5) NOT NULL,
  Last_Name CHAR(15),
  First_Name CHAR(15) )
```

Each CREATE TABLE statement gives the table's name, along with the name and data types of each of that table's columns.

Each table in each schema must have a unique name. It is possible, however, for two tables in two different schemata to have the same name. When that happens, you distinguish those

tables by referring to them with the qualified form *U.T*, where *U* is the name of the user who owns the schema and *T* is the table's name. So, if there were another Employees table in a different schema, you might refer to your table as USER1.Employees.

You refer to columns in a similarly qualified form, *T.C*, where *T* is the table name and *C* is the column name. (You can sometimes omit the *T* qualifier when the context makes it clear to SQL which column you want.) Thus, Employees.Last_Name and Dependents.Last_Name identify two of the fields in our example. We could still further qualify Employees, as in USER1.Employees.Last_Name, if there were a second Employees table in another schema.

We introduced two new elements in these examples: NOT NULL and UNIQUE. Any row can be missing the value for any column unless the definition of that column includes a NOT NULL qualifier. Because we wanted to force every row in both tables to include at least an employee ID, we made those columns NOT NULL. The UNIQUE qualifier on Employees.Employee_Id forces every row in the Employees table to have a unique employee ID. You can use this qualifier only on columns that are NOT NULL.

Other Commands

With the statements described above, you can define a simple ANSI SQL database. There are, however, a few other important DDL commands.

The CREATE VIEW statement lets you define

table. A view is a subset of the columns of a table and, optionally, a query that selects a subset of the table's rows. If, for example, we wanted a view that listed the employee IDs and last names of all employees who live in Florida, we would enter

```
CREATE VIEW Floridians ( Employee_Id, Last_Name )
AS SELECT Employee_Id, Last_Name
FROM Employees
WHERE State = 'FL'
```

Note that the SELECT statement defines a query that picks the rows we wanted.

Once you define a view, you can treat it almost as if it were another table. The only difference is that SQL doesn't let you update the rows of certain classes of views; basically, you can update rows in any view whose columns all come from a single table, as long as it includes all the NOT NULL columns from that table.

SQL's DDL also contains a statement, GRANT, which controls database security. The GRANT statement has the following form:

```
GRANT <operation> ON <table> TO <user>
```

In this statement, <operation> is one or more of the SQL DML verbs (such as SELECT or INSERT). For example, USER1 could let USER2 query the Employees table by entering

```
GRANT SELECT ON Employees TO USER2
```

As it stands, this statement doesn't let USER2 pass on this ability to other users. To add that ability, you must append the WITH GRANT OPTION clause:

```
GRANT SELECT ON Employees TO USER2 WITH GRANT OPTION
```

You can also take shortcuts. You can let a user do anything to a table by replacing <operation> with ALL. And you can open a table to all users by using PUBLIC instead of a user name.

After the Definition: DML

Once you've defined a database, you can begin working on it. SQL has four main DML verbs: INSERT, SELECT, UPDATE, and DELETE. All these verbs can work on more than one row at a time.

The SELECT statement is the heart of the language. It lets you query the database. Its result is essentially an unnamed, temporary relation that contains the data you requested. The SELECT statement follows this pattern:

```
SELECT <selection>
      <table_list>
      <_query>
```

<_query> is the list of fields that you want, and <table_list> is a comma-separated list of the tables that

you want to query. For example, to query the Dependents table, for exam-

```
SELECT First_Name
```

you can query the Dependents table for performing even this simple listing all the columns in a table

when you want them all, you can replace <selection> with an asterisk (*). Thus, another way to express the above query is as follows:

```
SELECT *
FROM Dependents
```

By default, SELECT will return to you all the rows that match the query criteria that you present, even if some of those rows are completely redundant. In our example, if two parents work together and the company stores each dependent row twice (once for each parent), the above query would return those redundant rows. To eliminate them, you add the DISTINCT qualifier:

```
SELECT DISTINCT *
FROM Dependents
```

If you want to be sure to retain those rows, you can use the ALL qualifier in place of DISTINCT, but ALL is the default.

Some queries naturally span several tables. If, for example, you wanted the first names of all dependents of employees in Florida, you would need to use the following, more complicated SELECT:

```
SELECT Dependents.First_Name
FROM Dependents, Employees
WHERE ( Employees.State = 'FL' )
AND ( Employees.Employee_Id =
      Dependents.Employee_Id )
```

This example illustrates several more options. First, you're retrieving from more than one table, so you must list both tables in the FROM clause. Next, because there's a First_Name field in both tables, you have to qualify which one you want. Finally, you're now using the <optional_query> clause. This clause can be far more complex than space permits us to cover fully here, but a few key portions are worth noting.

For a standard query, you first use the keyword WHERE and then give a Boolean expression that identifies the rows you want. That expression can contain groups of comparison clauses much like those of most programming languages, which you can separate and group by using AND, OR, and parentheses. The parentheses in the above example aren't necessary, but they make the query easier to read.

The comparisons in a WHERE clause can involve a field and a value, or two fields. In our example, the first comparison chooses employees whose state is 'FL'. The second comparison is more complicated; it performs what relational systems call a *join*. A join lets you choose matching rows in two different tables. In this example, we ask for all the Dependents whose Employee_Id column matches the Employee_Id column in any Employee record—in other words, the dependents of all employees. The SQL system puts these two clauses together so that you get only dependents of employees in Florida.

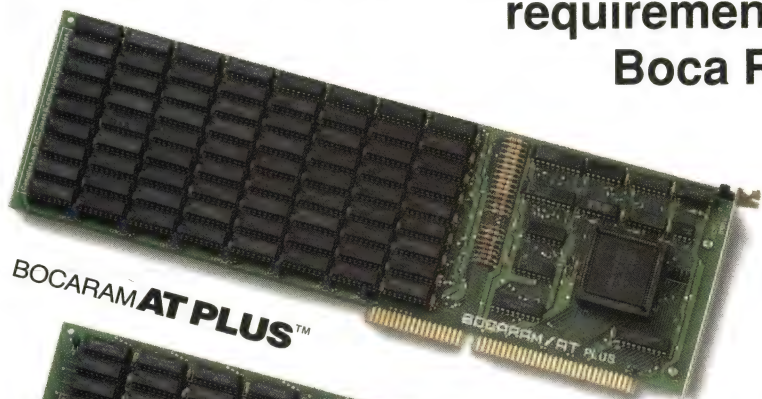
Joins can be very expensive because they can retrieve many rows; in this example, finding the dependents of all employees could take a lot of time. The SQL philosophy is that you should state the query you want and leave to the system the task of figuring out an efficient way to retrieve the data. In this example, it's more effective for the system first to find all employees in Florida and then to join those rows to their dependents' rows, rather than to do the join first.

The problem of determining how best to execute a SELECT

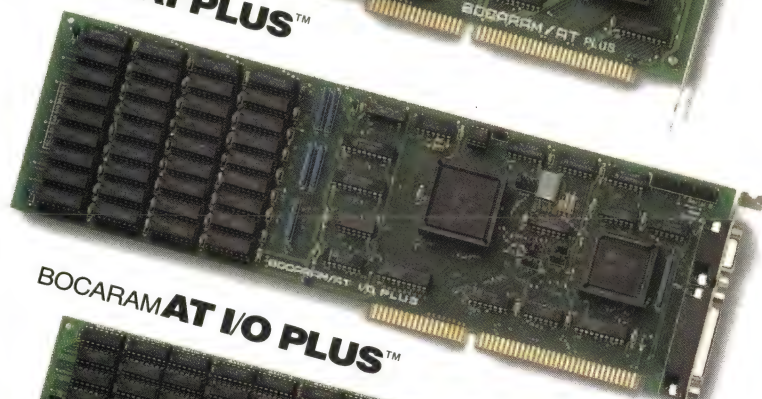
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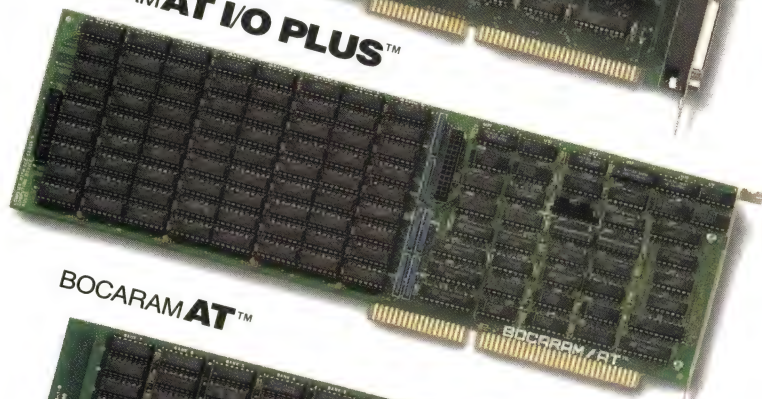
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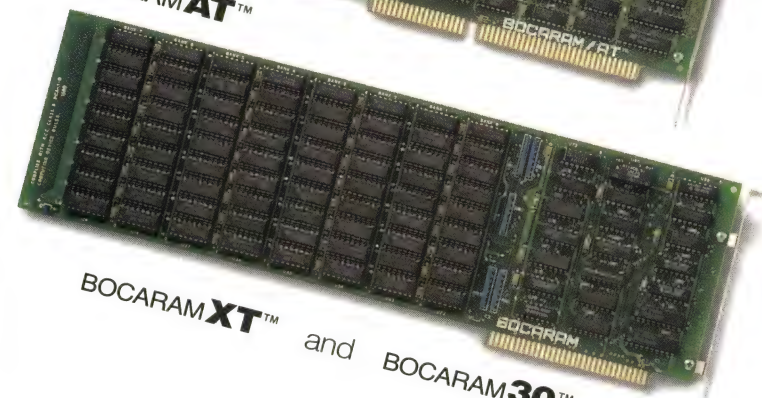
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query is called *query optimization*, and it's an area in which SQL vendors are constantly trying to best one another. Most SQL systems also have guidelines that help you frame your queries in a way that the system is most likely to execute efficiently, but those guidelines vary widely.

Our example will return the `First_Names` we wanted, but the order in which they will appear is unknown. We can control that order with the `ORDER BY` option. The query

```
SELECT Dependents.First_Name
FROM Dependents, Employees
WHERE ( Employees.State = 'FL' )
      AND ( Employees.Employee_Id =
            Dependents.Employee_Id )
ORDER BY Dependents.First_Name ASC
```

returns the first names in ascending order. Because `ASC` (for *ascending*) is the default in an `ORDER BY` clause, we could have omitted it here and produced the same result. To see the names in descending order, replace `ASC` with `DESC`.

There's much more to the `SELECT` statement; you can nest selects, group results, and compute functions like `MIN`, `MAX`, and `AVG` over the groups, and you can execute many other functions. You can also use more complicated comparison operators, including range checks and partial string matches.

Three other SQL verbs let you manipulate the rows in a table. You add new rows to a table with the `INSERT` statement. In its simplest form, you just give a table name and the values for the columns of the new row. The statement

```
INSERT INTO Dependents
VALUES ( 55816, 'Jones', 'Fred' )
```

creates a new dependent, Fred Jones, for employee 55816. Because SQL remembers the order of a table's columns, we don't need to include any column names. If you want to insert the column values in a different order, you can list the columns, after the table name, in that new order, as in

```
INSERT INTO Dependents ( First_Name, Last_Name,
                        Employee_Id )
VALUES ( 'Fred', 'Jones', 55816 )
```

You can also leave any columns null that the table's definition allows. To omit the first name from the new row above, use the `NULL` keyword:

```
INSERT INTO Dependents ( First_Name, Last_Name,
                        Employee_Id )
VALUES ( NULL, 'Jones', 55816 )
```

You can use a more complicated form of `INSERT` to insert multiple rows at once. This form uses a `SELECT` statement as the source of its rows. For example, if we had a temporary table, `Temporary`, whose definition had only `First_Name` and `Last_Name` fields, we could use the following `INSERT` statement to fill it with the names of all Florida employees:

```
INSERT INTO Temporary ( Last_Name, First_Name )
SELECT Last_Name, First_Name
FROM Employees
WHERE Employees.State = 'FL'
```

You can change values in specific rows with the `UPDATE` statement. `UPDATE` uses a `WHERE` clause just like the one in

`SELECT` to identify the row or rows that you want to change. For example, if the last name of employee 55816 changes to Jones-Smith, you can make that correction in all dependent records with the statement

```
UPDATE Dependents
SET Last_Name = 'Jones-Smith'
WHERE Employee_Id = 55816
```

The `DELETE` statement similarly uses a `WHERE` clause to identify the rows that you want to remove. To delete all dependents for employee 55816, enter

```
DELETE FROM Dependents
WHERE Employee_Id = 55816
```

Obviously, with this kind of power you have to be careful. If you leave off the `WHERE` clause, as in

```
DELETE FROM Dependents
```

you delete all the rows in the `Dependents` table. The table definition itself remains, but the rows are gone. Fortunately, SQL also defines some transaction controls that provide a way to undo many errors.

A SQL transaction is a series of one or more commands that can end either normally or abnormally. If a transaction ends normally, all its commands are done. If a transaction ends abnormally, then none of its commands are done. The SQL system guarantees that the database is never in an inconsistent state (i.e., a state where one or more transactions are partially done).

To end a transaction normally, we use the verb `COMMIT`. `COMMIT WORK` completes the current transaction. It also effectively starts a new transaction; you're always working in a transaction.

Its counterpart is `ROLLBACK`; `ROLLBACK WORK` cancels all the database changes of the current transaction. The database then appears as it would if the transaction had never occurred. By using `ROLLBACK` right after our earlier accidental deletion, you could undo that mistake.

SQL in Programming Languages

The SQL standard concentrates on making the SQL commands work with traditional programming languages. It offers two ways to do this.

The less frequently used approach is called the *module language*. In it, you write a module that consists of a header and a series of procedures. The procedures contain only parameter definitions and one or more SQL statements.

For example, a module that lets us perform our simple `DELETE` might be

```
MODULE Deletion_Work LANGUAGE PLI AUTHORIZATION
USER1
PROCEDURE Delete_Deps
SQLCODE;
Emp_Id DECIMAL(5);
DELETE FROM Dependents
WHERE Dependents.Employee_Id =
      Emp_Id;
```

`Emp_Id` is a parameter that will contain the ID of the employee whose dependents we want to delete. Note the special

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parameter `SQLCODE`; SQL requires this parameter in every procedure. When the procedure finishes, `SQLCODE` will contain the result of the operation—positive for success, and negative for failure.

We could then call this procedure from a program in the usual way. In PL/I, it would be

```
CALL Delete_Deps ( return_code, 55816 );
```

Real modules would, of course, contain many more complicated procedures, but they would follow the same framework as our example.

The big advantage of the module language is that it requires very little from the host programming language. A new SQL-specific compiler can compile the module into an appropriate form, and then the host language needs only to be able to call and link to the module's procedures. Most systems support some form of cross-language procedure calls, so these requirements are easy to meet.

However, the module language is not very satisfactory, because you must write and compile all your SQL statements separately. To provide a more unified programming environment, the SQL standard also includes a series of appendixes that define *embedded* versions of SQL for several languages.

An embedded version is designed to fit more smoothly into the language itself. It would be possible for vendors to implement embedded SQL by changing the compiler, but, instead, most provide preprocessors that convert embedded SQL into more-primitive calls that the underlying database system understands.

Embedded SQL lets you put SQL statements in the middle of ordinary code by prefixing those statements with `EXEC SQL`. For example, we could use embedded SQL to replace the above `CALL` to the SQL procedure with this code fragment:

```
EXEC SQL DELETE FROM Dependents
      WHERE Dependents.Employee_Id = 55816;
```

Most SQL vendors today offer embedded SQL for one or more languages.

The one remaining problem for SQL in programming languages lies in dealing with multiple rows. SQL solves this problem with a simple technique borrowed from traditional file processing: It defines a *cursor* that marks the current position in the group of result rows.

You declare a cursor by giving the `SELECT` statement that defines it. A cursor for the example that selected the first names of dependents of Floridian employees would look like the following:

```
EXEC SQL DECLARE C1 CURSOR FOR
      SELECT Dependents.First_Name
      FROM Dependents, Employees
      WHERE ( Employees.State = 'FL' )
            AND ( Employees.Employee_Id =
                  Dependents.Employee_Id )
      ORDER BY Dependents.First_Name ASC ;
```

You can also include variables in these definitions, as long as you first declare those variables in a special SQL declaration section. To make this example work for any state, you could use the following:

```
EXEC SQL BEGIN DECLARE SECTION;
      DCL state CHAR(2);
```

```
      DCL name CHAR(15);
EXEC SQL END DECLARE SECTION;

EXEC SQL DECLARE C1 CURSOR FOR
      SELECT Dependents.First_Name
      FROM Dependents, Employees
      WHERE ( Employees.State = :state )
            AND ( Employees.Employee_Id =
                  Dependents.Employee_Id )
      ORDER BY Dependents.First_Name ASC;
```

The colon in front of `state` in the `SELECT` statement identifies `state` as a variable. (We'll consider the other variable, `name`, below.)

Once you've defined a cursor, you treat it much like a file. First you open it, and then you can cycle through its rows until there are no more. You could retrieve all the Floridian dependents using the above cursor in only a few statements, as the following pseudocode demonstrates (we ignore error checking here to save space).

```
state = 'FL'; /* pick the state
              you want */
EXEC SQL OPEN C1; /* tell SQL to
                  perform the query */
DO WHILE <more employees> /* read all rows
                          the query retrieved */
EXEC SQL FETCH C1 INTO :name; /* now do what
                               you will with
                               the name you
                               retrieved */

END;
EXEC SQL CLOSE C1;
```

You can treat these three `EXEC SQL` options—`OPEN`, `FETCH`, and `CLOSE`—much like typical file open, read, and close statements.

Once you're on a record, you can change it with `UPDATE` or delete it with `DELETE`; both commands have embedded SQL versions that work on the current cursor row. Again, this is much like traditional file operations. You finish your work in the usual SQL way, with a `COMMIT` or `ROLLBACK` (prefixed, of course, by `EXEC SQL`).

The Rest of the Story

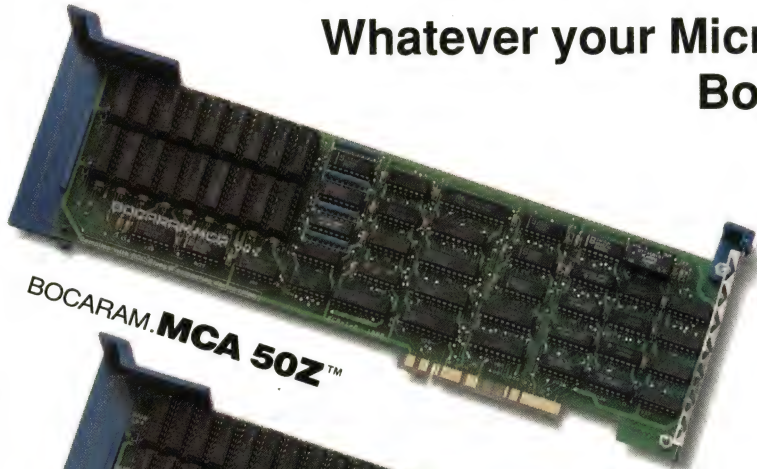
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SQL lets an organization use a single language to link its microcomputer, minicomputer, and mainframe databases. It is also the language that virtually all the announced LAN database servers support. As such links to host and server databases become more important, SQL will emerge as the second microcomputer database language standard. ■

Mark L. Van Name, a BYTE consulting editor, and Bill Catchings are independent computer consultants and freelance writers based in Raleigh, North Carolina. You can reach them on BIX as "mvanname" and "wbc3," respectively.

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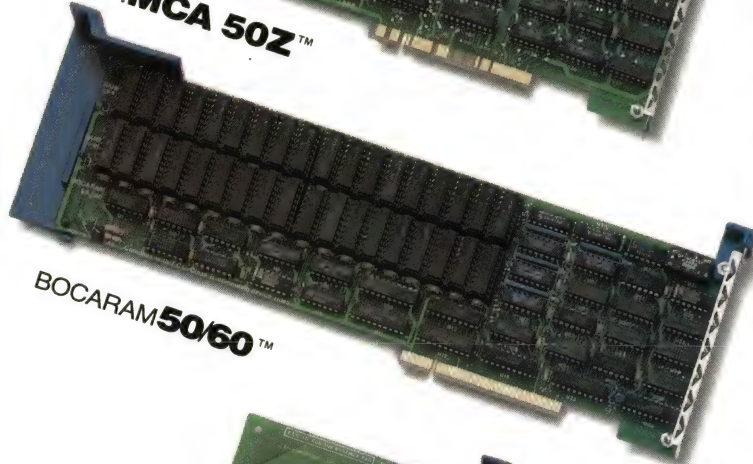
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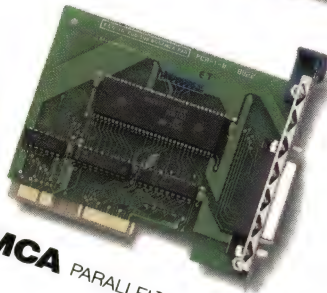
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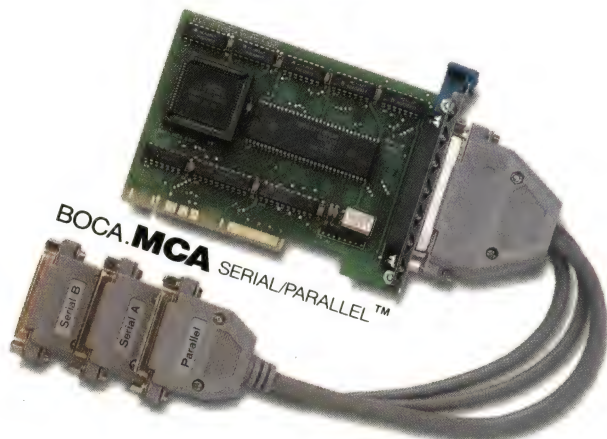


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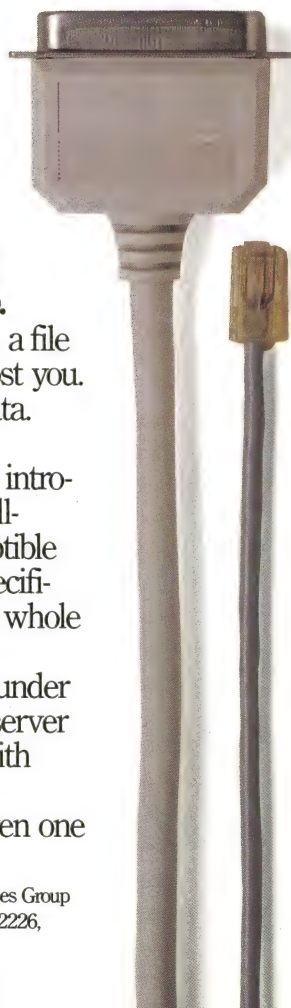
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UNIX FILENAMES FOR TURBO PASCAL

Metaname is a simple unit that provides the flexibility of Unix filenames for Turbo Pascal programs

Jim Kerr

Most operating systems permit the use of wildcard characters, or *metacharacters*, in commands that make reference to files. Metacharacters allow you to refer to certain files as a group, rather than having to specify the individual filenames. Unix, however, provides a more sophisticated way of specifying filenames than DOS does.

MS-DOS has just two metacharacters, * and ?. The * character represents any sequence of zero or more characters, and ? represents any single character. (MS-DOS filenames cannot contain the characters " \ [] : ! | < > - + = ; , * and ?.)

In the Unix operating system, there are five metacharacters: * ? [] -. The * character matches any sequence of zero or more characters, including the period, and can be followed by other characters. The symbol ? matches any single character. The remaining three metacharacters are used to define *character classes*. Character classes are just sets of characters, and they're described by a syntax similar to that used for sets in Pascal. For example, the character class [akp-z6] in-

cludes the characters a, k, p through z (inclusive), and 6.

Note the special meaning of the hyphen in this example. When it appears in a character class between two other characters, the hyphen is interpreted as a range indicator. The hyphen may also be interpreted literally. This occurs if it appears as the first or last character in a character class, or if it appears outside

the character-class specification. For example, the character class *-* matches all filenames that contain a hyphen, while ?[-0-9]* matches all filenames that have a hyphen or a digit in position 2. The hyphen has a sort of dual nature; depending on the context, it may be interpreted as either a metacharacter or a literal. For the sake of convenience, I'll refer to file masks containing metacharacters as *metacharacter expressions*.

Given a metacharacter expression for filenames, how can you tell if a particular filename matches the pattern? I'll discuss an algorithm to answer this in the next section and then describe a Turbo Pascal unit that implements the file-matching algorithm. Using the Metaname unit (described in detail later), a Turbo Pascal program can use Unix metacharacters in filename searches. This is illustrated in a simple demo program that accompanies the source code for this article.

Finite Automata

In automata theory, a language is defined as any collection of strings. In this context, a metacharacter

continued



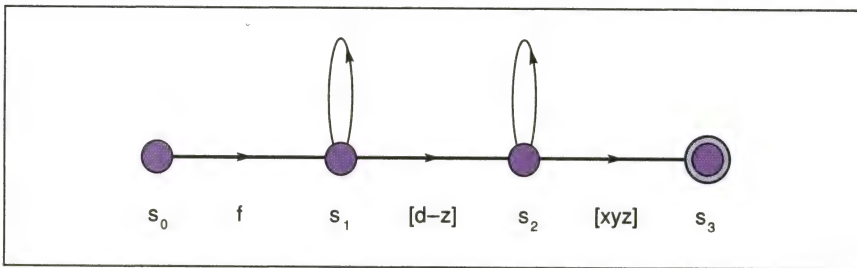


Figure 1: A nondeterministic finite automaton that accepts the metacharacter expression $f*[d-z]*[xyz]$.

Table 1: Operation of the finite automaton in figure 1 on the input string fuzzy.

Unread input	State set
fuzzy	{0}
uzzy	{1}
zzy	{1,2}
zy	{1,2,3}
y	{1,2,3}
—	{1,2,3}

expression such as $f*[d-z]??$ describes a language—namely, the language of all strings that fit the implied pattern. To determine whether a filename is in the language L associated with a metacharacter expression, I'll use a language-recognition device called a *finite automaton* or *finite state machine*. This device takes a string as input, performs some computations, and then signals whether or not the string is in the language L .

Were it not for the metacharacter $*$, filename matching would be easy. To determine whether a filename matches the expression $f[aeiou]?$, for example, you would only need to check that the filename begins with f , contains a vowel in the next position, and terminates after the third character.

Once you include $*$ in the metacharacter repertoire, however, file matching becomes more complicated. To see why, consider what happens if the metacharacter expression is $f*[d-z]*[xyz]$ and the filename is *fuzzy*. It's easy to see that the leading characters match, but what about the second character? Should the u be matched to the metacharacter $*$, or should it be assigned to the character class $[d-z]$? When considering how to match the third character, z , you again have two options. You have to be prepared to manage several simultaneous decision paths when seeking a possible match. Understanding finite automata is helpful in understanding the element of

nondeterminism introduced by the metacharacter $*$.

Perhaps the best way to illustrate how a finite automaton works is through an example. Figure 1 shows the finite automaton for the metacharacter expression $f*[d-z]*[xyz]$. The automaton consists of states, labeled s_0 through s_3 , and labeled arcs connecting the states. The labels on the arcs indicate which characters permit a transition from one state to the next. In any automaton, there are two special states. State s_0 is called the *start state*, because this is the state in which the automaton begins operating. State s_3 is the *final state*. In a certain sense, the final state represents the goal of the computation. Most often, the start state is indicated with an arrow, while the final state is drawn as a double circle.

The process of running a finite automaton is something like navigating through a maze. In a maze, there are prescribed start and stop positions, and restrictions on which direction you can go from any point. Moreover, it's not always clear which choice of direction will bring you to the desired goal. In a finite automaton, there are designated start and final states, and restrictions on when you can move from one state to another. As in a maze, there may be several states to move to under some circumstances, and the proper choice may become clear only in retrospect.

Initially, the automaton is in state s_0 .

Thereafter, characters are read from the input string one at a time. Each time a character is read, the automaton makes a transition from some state s_i to some state s_j , if the arcs permit it. For a given input character, there may be no legal transitions, exactly one, or more than one.

For example, if the automaton is in state s_1 and the input character is q , the machine can either stay in s_1 (using the arc labeled $*$) or move to s_2 . The operation of the automaton is not determined solely by the input string, because the machine can sometimes "choose" which state to enter next. For this reason, automata such as this are referred to as *nondeterministic finite automata*.

If there's some way to move from the start state to the final state such that the final state is entered after the last input character has been read, the finite automaton "accepts" the string; otherwise, it's rejected. For the automaton in figure 1, with the input string *fuzzy*, the proper choice of transitions yields the sequence $s_0 \rightarrow s_1 \rightarrow s_1 \rightarrow s_2 \rightarrow s_3$. Several other sequences are possible—for example, $s_0 \rightarrow s_1 \rightarrow s_1 \rightarrow s_1 \rightarrow s_1 \rightarrow s_2$ —but none of these leave the automaton in state s_3 when all input has been consumed.

For a given automaton and input string, how can you tell whether there's a sequence of transitions that takes the ma-

Running a finite automaton is like navigating through a maze.

chine from its start state to its final state? One solution involves keeping a list of all the possible states the automaton can be in, on the basis of the input characters read thus far. If this state list contains the final state after all input has been read, then there must be some sequence of transitions that takes the automaton from the start state to the final state, and the string should be accepted.

If the final state doesn't appear in the final state list, the string is rejected. Table 1 illustrates this process for the automaton that is shown in figure 1. Since the order of states in the list isn't important, you can use a set representation for

continued

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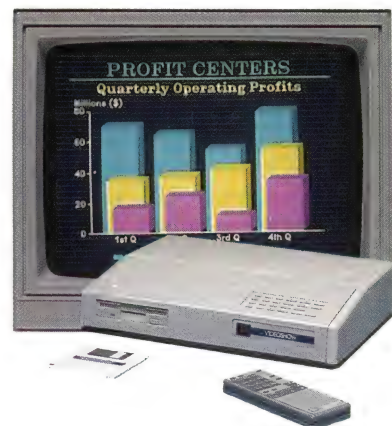
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Regular Expressions

A *regular expression* is a compact notation for describing sets of strings that have a pattern to them. These patterns are formed by taking primitive strings, such as single characters and the empty string, and repeatedly applying them to operations of alternation, concatenation, and repetition.

Regular expressions are formed from the combination of metacharacters with standard characters. For example, the expression $(\backslash+|-)?[0-9]+\backslash.[0-9]^*$ matches a decimal number with an optional sign and optional fractional part, and the expression $(AB)^+C$ matches ABC, ABABC, ABABABC, and so on.

The Unix editors and utilities use regular expressions extensively. In fact, there's a utility called *grep* (for global regular-expression printer) that does nothing more than find all strings in a file that match a given regular expression. Unfortunately, the way regular expressions are used under Unix is somewhat inconsistent.

The Unix shell—the part of the operating system that resides between the kernel and the user—interprets regular expressions differently from *grep*, text editors, and other text-based utilities. For example, if you invoke the file-list-

ing utility *ls* with *ls [ab]**, the shell interprets $[ab]^*$ as $(a \cup b)(\text{anything})^*$, the set of strings that begin with *a* or *b*. But *grep* interprets $[ab]^*$ as the regular expression $(a \cup b)^*$; that is, as strings of length zero or greater that consist exclusively of *a*'s and *b*'s. Since every line in a file contains the zero-length member of this set, the *grep* command will print out every line in the file. When using regular expressions under Unix, it's important to keep in mind whether you're dealing with the shell or with a utility.

Formally Defined

To form a regular expression, begin with a set of characters Σ , called an alphabet. The regular expressions over alphabet Σ are defined as follows:

1. The empty string ϵ is a regular expression. Any single character a in Σ is a regular expression.
2. If r is a regular expression, so are r^* and (r) .
3. If r_1 and r_2 are regular expressions, so are $r_1 r_2$ and $r_1 \cup r_2$.

Associated with each regular expression r is a language, denoted by $L(r)$.

The definition of $L(r)$, like the definition of regular expressions, is recursive:

1. $L(\epsilon) = \{\epsilon\}$, the language consisting of the empty string. Also, $L(a) = \{a\}$ for each a in Σ .
2. $L(r^*) = (L(r))^*$. The expression on the right (the Kleene closure) is formed by concatenating zero or more strings in $L(r)$. Parentheses around a regular expression don't affect the language it denotes, so $L((r)) = L(r)$.
3. $L(r_1 r_2) = L(r_1)L(r_2)$, and $L(r_1 \cup r_2) = L(r_1) \cup L(r_2)$. The first relation says that $L(r_1 r_2)$ is obtained by constructing all strings of the form $s_1 s_2$, where s_1 is in $L(r_1)$ and s_2 is in $L(r_2)$. The second says that $L(r_1 \cup r_2)$ is the union of the languages $L(r_1)$ and $L(r_2)$.

It's customary to give $*$ the highest precedence in regular expressions, concatenation the next highest, and union the lowest. The usual precedences can be overridden by using parentheses. Under this convention, you have $L(a \cup bb^*c) = L(a) \cup L(b)L(b)^*L(c) = \{a, bc, bbc, bbbc, \dots\}$, while $L((a \cup b)b^*c) = \{ac, bc, abc, bbcc, \dots\}$.

states instead of a list, as is done here. Since the final state, s_3 , is in the last state set, the string *fuzzy* is indeed accepted by this automaton.

Now that I've described how a finite automaton operates, I should discuss how to construct an automaton from a metacharacter expression. For the purpose of this discussion, I will refer to the parts of a metacharacter expression—the symbols $*$ and $?$, character classes, and single characters not in a class—as *subexpressions*. The algorithm to build the automaton goes as follows:

1. Begin with a start state s_0 . Let $n = 0$.
2. Read the next subexpression from the metacharacter expression. If it's a $*$, draw an arc labeled $*$ from s_n to itself. Otherwise, create a new state s_{n+1} , draw an arc labeled with the subexpression from s_n to s_{n+1} , and increment n by one unit.
3. Repeat step 2 until the entire metacharacter expression has been read. State s_n then gives the final state of the automaton.

This algorithm only applies to finite automata that recognize metacharacter expressions. These expressions, and the languages they generate, are but a small subclass of the so-called *regular expressions* and *regular languages* (see the text box "Regular Expressions" above). Some regular languages are quite complex, and constructing finite automata that recognize them is no simple matter. The relationship between finite automata and regular languages is well understood, however, and there are algorithms to answer almost every question relating to them. References 1, 2, and 3 contain comprehensive discussions of automata and languages.

Implementation

The algorithms given so far for automaton construction and operation are simple enough to master without much practice. They're also simple enough to easily implement in software. Moreover, there is a direct way to represent this sort of finite automata in Pascal. One consequence of the algorithm given earlier is that no state in the machine will have more than

two outgoing arcs. Also, the automaton cannot have more than 12 states, since DOS filenames are limited to 12 characters. This means that you can represent the automaton as an array of records:

```
var Arcs : array[0..11] of
    record
        set1, set2 : set of char;
        NextState1, NextState2 :
            0..11
    end;
```

The fields *set1* and *set2* are the sets of characters associated with the outgoing arcs from a particular state; *NextState1* and *NextState2* are the states that these outgoing arcs lead to. For the finite automaton shown in figure 1, you have

```
Arcs[1].set1 := AllChars;
Arcs[1].set2 := [d..z];
Arcs[1].NextState1 := 1;
Arcs[1].NextState2 := 2;
```

where *AllChars* is the entire set of ASCII characters. If a state has only one

continued

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outgoing arc, then set2 is empty. The final state has no outgoing arcs, so both set1 and set2 are empty for the final state.

Having decided what data structure to use for the automaton, you can then write procedures to construct and run the automaton. The procedure `MakeAutomaton` accepts a metacharacter expression as input and generates as output a finite automaton that accepts the associated language. Procedure `Accept` takes a filename as input and returns a Boolean value (`true` or `false`, indicating whether the automaton created by `MakeAutomaton` accepts the filename).

I've written a Turbo Pascal 4.0 unit called `Metaname`, in which I have assembled the procedures `MakeAutomaton`, `Accept`, and some required support code. Actually, `MakeAutomaton` and `Accept` don't appear in the interface portion of this unit at all. Since the only purpose in constructing automata is to match filenames with metacharacter expressions, there's no good reason to even mention automata in code that uses `Metaname`.

The user should be able to specify a wild-card expression and use the unit to

There is a direct way to represent this sort of finite automata in Pascal.

find matching filenames. To this end, I have written two procedures, called `MatchFirst` and `MatchNext`. These procedures have the same calling sequence as the Turbo Pascal file search procedures `FindFirst` and `FindNext`, but they accept Unix metacharacter expressions rather than just DOS wild cards. The interface section of the `Metaname` unit is as follows:

```
interface
uses DOS;
Procedure MatchFirst(Path:
String;
Attr: Word; var S:
SearchRec);
```

```
Procedure MatchNext(var S:
SearchRec);
```

The first argument of procedure `MatchFirst` specifies the path and metacharacter expression you want to match. A legal value for the variable `Path` might be `TP4\PROGRAMS*PGM[0-9]*`. The `Path` string doesn't have to be uppercase; `MatchFirst` performs case conversion automatically. The variable `Attr` gives the attribute of the file you're seeking: read-only, archive, directory, or whatever. If a match is found, information about the matching file is returned in the record variable `S`. The record type `SearchRec` (which is declared in the standard unit `DOS`) contains fields for the filename, size, date of creation, and file attributes.

If `MatchFirst` succeeds, you can invoke the procedure `MatchNext` to find the next matching file. These procedures return error codes through the DOS unit variable `DosError`. If the path argument in `MatchFirst` references a nonexistent directory, `DosError` is set to 2. If either `MatchFirst` or `MatchNext` fails to find a

continued

QUERY

select report graph histogram

Display fields from 2 tables by typing, on DOS prompt

```
C> SELECT ID,PC.NAME,SPEED FROM SPEED,PC WHERE ID= PC.ID
```

- wildcard & metacharacter in filter
- 1-1 or 1-many relation. multiple relation
- readonly,frozen,calculated field. running total
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match, `DosError` is set to 18. If no error occurs, `DosError` is 0. To find all matching filenames, call `MatchFirst`, and if it returns without error, call `MatchNext` until `DosError` is nonzero.

Using the Metaname Unit

To use Unix metacharacters in a Turbo Pascal 4.0 program, you need only include the `Metaname` and `DOS` units in the `uses` clause at the beginning of the program. After that, you can invoke `MatchFirst` and `MatchNext` in the same way that you would call `FindFirst` and `FindNext`.

There are some points to keep in mind when using the `Metaname` unit. To maintain strict compatibility with Unix file operations, the metacharacters `*` and `?` match all characters when used in a filename search, including the period. If you want `MatchFirst` and `MatchNext` to be upwardly compatible with DOS wildcard matching, you should include the statement `{ $DEFINE DOSCOMPAT }` near the beginning of the `Metaname` unit. This will exclude the period from the set of characters that `*` and `?` match.

Also important to know is that the

`Metaname` unit doesn't perform any syntax checking on metacharacter expressions. If you try to match filenames to something like `][-?`, be prepared to suffer for your transgressions.

When using character classes, remember that the first and last characters in a range obey ASCII ordering. If you specify a class like `[16-24]`, you won't get the numerals 16 to 24, but rather the digit 1, the range 6-2 (whatever that is), and the digit 4. On most Unix systems, a range in which the second character has a lower ordinal number than the first is processed by including the two characters into the class. With this interpretation, the class `[16-24]` is the same as `[1246]`. This approach is used here.

If you wish, you can use the code in `Metaname` to perform string matching on objects other than filenames. If you decide to do this, you will have to change the value of the `MaxStates` variable accordingly, and you will need to modify the `getchar` function if you want to enable case sensitivity.

With a modest amount of programming effort, you can write stand-alone programs to copy, move, delete, or list

groups of files described by Unix metacharacter conventions. Once you've become accustomed to Unix file conventions, you may not want to move back to DOS wild cards again! ■

Editor's note: *Metaname* is available in a variety of formats. See page 3 for details.

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Jim Kerr is a former mathematics professor who is now studying computer science at the University of California at Santa Cruz. His principal interests are compiler design and language theory. He can be reached on BIX c/o "editors."

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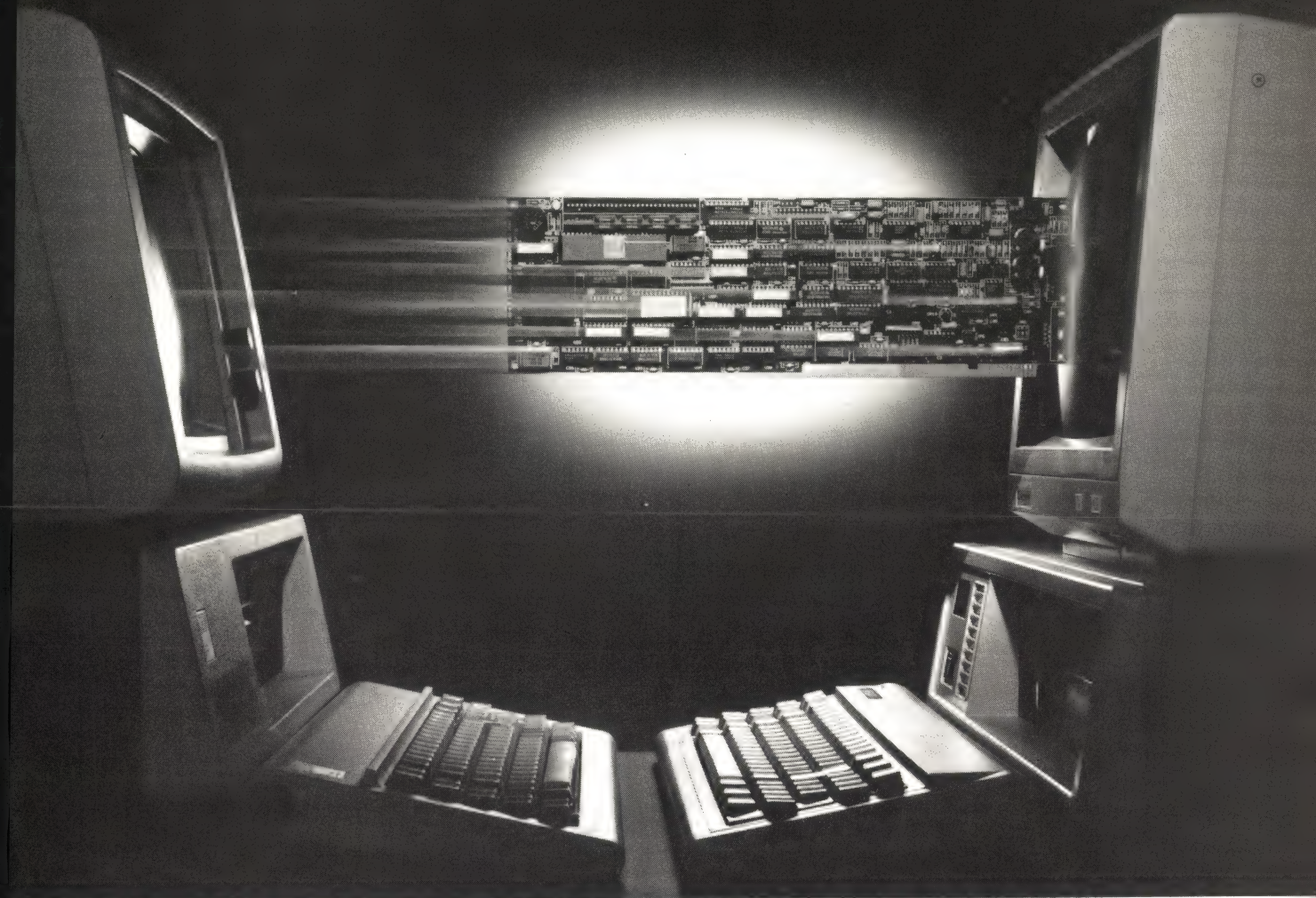
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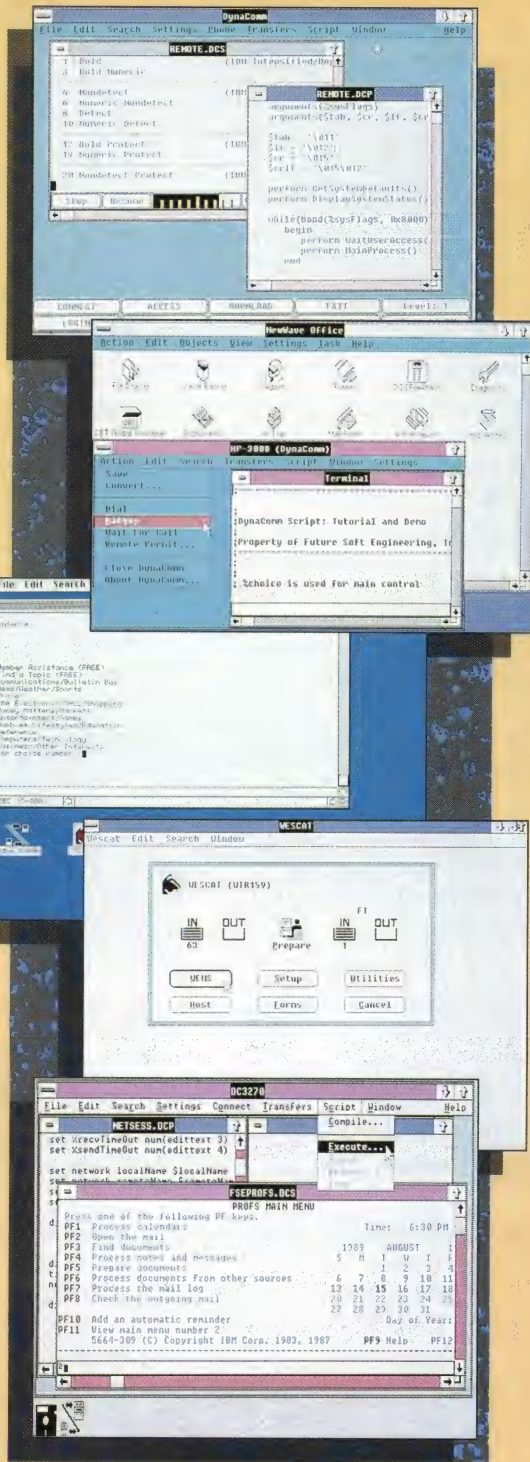
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WHICH LAN?

Understanding the strengths and weaknesses of the popular LAN connection options helps you get the system that fits your needs

Richard Watson

LANs are spreading like wildfire because they offer computing power that rivals that of minicomputer and mainframe installations at a fraction of the cost. When choosing a LAN, however, you have to take care that you don't get burned.

While the business benefits of LANs are numerous, so too are the connection options available. You can choose from over 20 network operating systems that work with hardware from more than 60 ARCnet, 50 Ethernet, and 20 Token Ring vendors. The key to simplifying your choice is to acquire a good understanding of the basic LAN technologies and the benchmarks used to measure them. This article presents an overview of the most common LAN connection hardware and outlines how you should evaluate a LAN.

Roots of Connectivity

Linking computers to share information is nothing new. The technology for most of today's LANs was created in the 1970s by minicomputer companies. As with most new technologies, the absence of standards led vendors to develop proprietary answers to

problems of connectivity.

While many connection solutions exist, only a few enjoy widespread support in today's microcomputer LAN market. Two of the more popular—ARCnet and Ethernet—are minicomputer connection solutions that have become standards in the LAN market. A later arrival on the scene is Token Ring, which can be considered a third-generation pro-

ocol and connection design. Backed by IBM, Token Ring is expected to rival Ethernet in the Fortune 1000 market.

Following Protocol

Selecting the proper LAN hardware has a direct impact on the performance and flexibility of the final LAN configuration. ARCnet, Ethernet, and Token Ring all have advantages and disadvantages you must consider in selecting equipment appropriate to you. What may be applicable for one implementation may not be the best choice for another.

Understanding some basic design aspects of each protocol is important for making informed judgments. Table 1 summarizes ARCnet, Ethernet, and Token Ring.

ARCnet

Datapoint Corp. originally developed ARCnet to permit Datapoint accounting equipment to exchange data in real time. Because Datapoint controls the hardware specifications and protocols of ARCnet, the microcomputer LAN version is virtually identical to the minicomputer implementation. The popularity of ARCnet in LANs today is a result of the simplicity of its

continued



Table 1: Prices reflect the average retail cost of one board and one driver—they do not reflect the cost of other components of the LAN.

LAN FEATURES AND SPECIFICATIONS						
Protocol	Transfer rate (megabits per second)	Maximum packet size (bytes)	Cost per connection	Access	Media types	Attributes
ARCnet	2.5	512	\$200	Token-passing	Coaxial, unshielded twisted-pair, fiber-optic	Inexpensive; reliable; broad vendor support
Ethernet	10	1.5K	\$400	CSMA/CD	Thin/thick coaxial, unshielded twisted-pair	Fast; broad vendor support; IEEE standard
Token Ring	4/16	4K	\$400/\$700	Token-passing	Shielded/unshielded twisted-pair	Extensive features; IBM support; IEEE standard

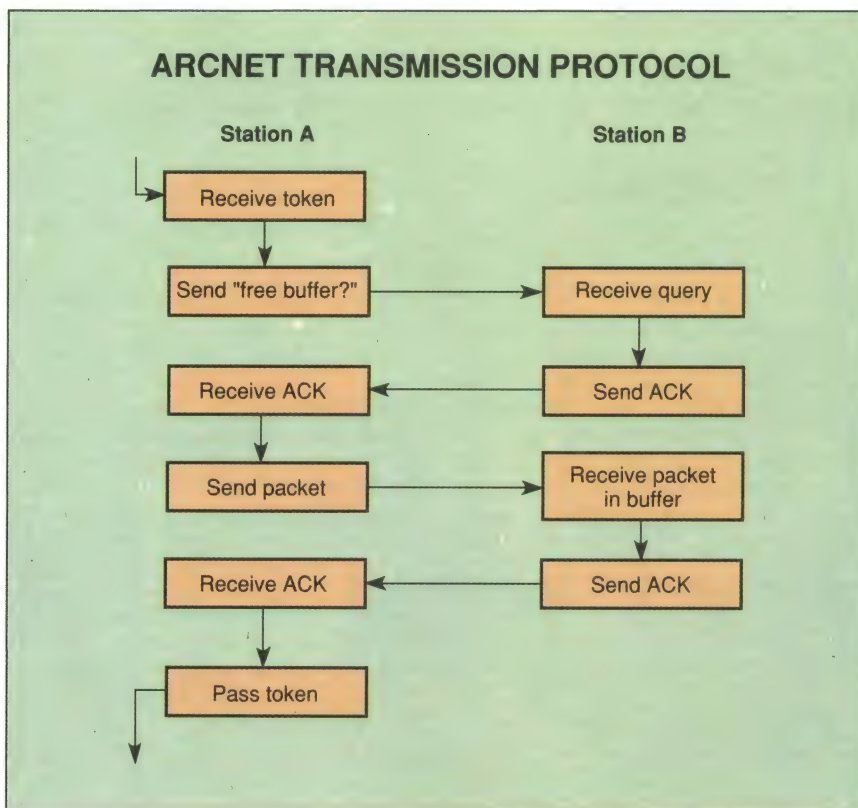


Figure 1: The "free buffer?" query helps ensure the reliability of ARCnet data transfers.

maintenance and low cost per node.

ARCnet uses a token-passing protocol implemented with a combination of dedicated communication controllers and hybrid interface components. ARCnet's basic star, or hub, topology and straightforward node configuration make it easy to install and debug. You can assign a network node one of 255 unique addresses by setting the configuration switches on the network interface card.

The ARCnet protocol is simple. On power-up, each node determines its

order on the node list. The token starts at the node with the lowest station ID, which either initiates communication or passes the token to the next-higher numeric station. When a station with the token wants to transmit data, it initiates the ARCnet transmit protocol.

Before transmitting, a station must ensure that the target station has a buffer available to receive the next packet. It transmits a "free buffer?" inquiry to the destination station. If the destination has a buffer available, it sends an acknowl-

edgment (ACK); the sending station then transmits the packet (see figure 1). If no buffer is available, the destination station returns a negative acknowledgment (NAK). Most ARCnet adapters have 2K-byte buffer memories, which hold four packets. This limitation can cause network performance to suffer when a busy node has no free buffers. In particular, a central server will often indicate a "no buffer" condition under heavy network traffic conditions.

After transmitting or receiving a negative acknowledgment, the sending station passes the token. Having built-in hardware support that helps ensure reliable packet delivery differentiates ARCnet from other LANs.

Adding and subtracting nodes is simple with ARCnet. Anytime the addition or subtraction of a node changes the sequence of active-node IDs, the network halts data transfer operations and reconfigures the network. These processes require only several hundred milliseconds to complete, but the network is down for this time. Thus, a network adapter that fails sporadically can bring the network to a standstill.

Ethernet

Developed by Xerox in cooperation with Digital Equipment Corp. and Intel to interconnect DEC minicomputers, Ethernet has become a popular LAN for microcomputers. It is noted for superior performance and wide vendor support.

Ethernet's dialogue on the network is much simpler than that of ARCnet because it supports larger buffers and CSMA/CD architecture. Unlike token-passing architectures, CSMA/CD places no restrictions on when data is transmitted; any station can transmit at any time. When two or more stations transmit data simultaneously, a collision occurs that can corrupt the data from each

station. The data-link layer detects collisions and resolves the contention by having each station wait for a random period before retransmitting (see figure 2).

Severe problems can occur on a CSMA/CD network when an adapter begins to fail and "jabbers" constantly. In this case, the network will be flooded with junk transmissions, causing almost constant collisions. To resolve this type of problem, the failing adapter must be removed as soon as it is identified.

Token Ring

Token Ring was developed by IBM in the early 1980s and is defined by the IEEE 802.5 standard. It was designed to support a broad variety of host machines, including mainframes as well as smaller computers such as PCs. Token Ring uses a token-passing technique that ensures a flat performance curve, regardless of the volume of traffic on the network (see figure 3). The Token Ring multiple-access-control-level protocol is richer in its node addressability than is ARCnet (48 bits versus 8 bits). It also has integrated routing and priority mechanisms that let you optimize any configuration. Token Ring has no data-link mechanism for assuring that the destination node has a receive buffer available; this is handled at higher levels by software.

Architectural Comparisons

Token-passing adherents and fans of CSMA/CD have a nearly religious devotion to their favorite access method. The "token-passers" are quick to point out that a CSMA/CD architecture can theoretically be brought to its knees by the collision arbitration scheme. On the other side, the "collision detectors" note that token-passing architectures are penalized in a client-server configuration where the predominant flow of data is from the server to the client nodes. The server must wait its turn while the workstations process the token; hence, token passing is deterministically slow.

In reality, both architectures suffer under heavy loads. A heavily loaded CSMA/CD network experiences performance degradation due to the increased number of collisions. Similarly, a token-passing network begins to suffer in a heavily loaded environment due to full buffers at busy receiving stations. This situation is an especially serious one for ARCnet installations because most adapters can buffer only four packets.

The only generalization that you can make based on architecture is that, although both collision detection and token

continued

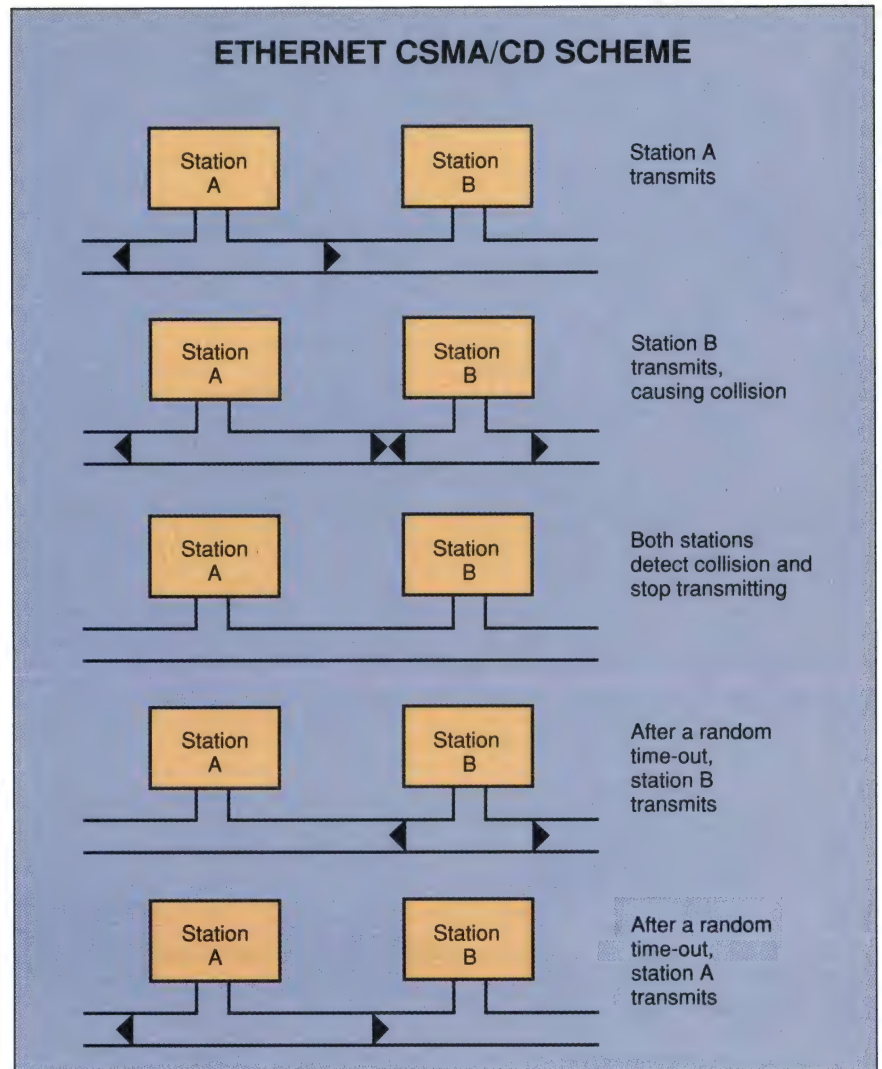


Figure 2: Stations detect collisions by listening for their own packets. If a packet is garbled, a collision is assumed.

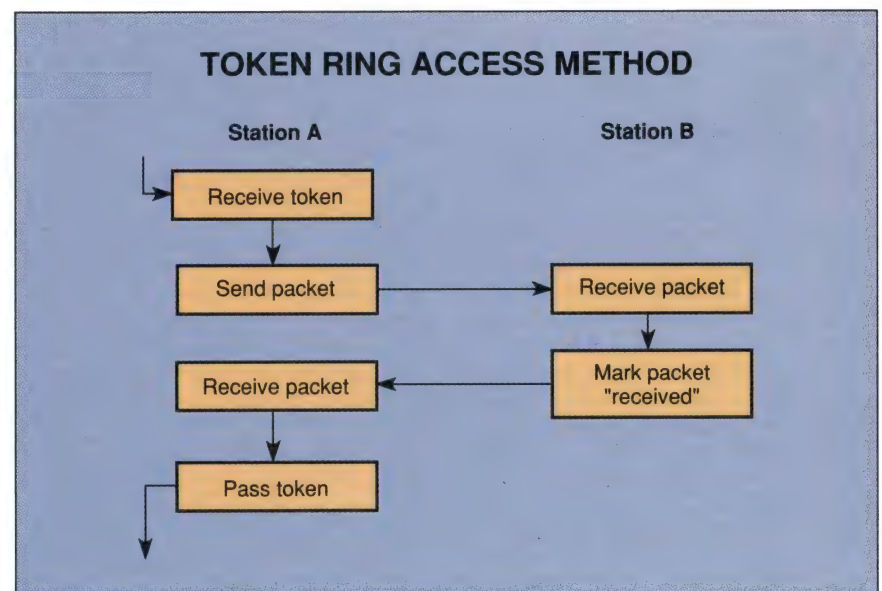


Figure 3: Token Ring is relatively simple at the physical and data-link layers, thus minimizing the traffic needed to establish communications.

LAN Yardsticks

The goal of a LAN benchmark is to determine a single performance index for a LAN implementation. With LANs, however, it is important to understand that many components from different vendors contribute to the generation of a performance metric. To achieve optimum performance, you'll have to configure your system with components from many vendors.

You can simplify the problem of measuring the performance of a multivendor LAN configuration by ranking the components in the order of their impact on LAN performance in relation to the target application environment. In a database environment, for example, the record-locking mechanism is likely to be the most significant factor in network performance. Thus, you can optimize performance by selecting fast disk drives and by configuring servers and workstations with as much cache memory as possible.

Listed below, in the order of their impact, are the factors that determine the performance of a generalized LAN implementation.

1. Multiple access control (record locking)
2. Hardware configuration
3. Network operating-system inefficiency
4. Application inefficiency
5. Driver/network interface card inefficiency
6. DOS inefficiency
7. Protocol overhead

Applications Impact

To a great extent, the observed performance in any configuration depends on the type of application. For applications such as word processing, you will observe virtually no performance difference at an individual node regardless of the size of the network. For a database application, the observed performance will be greatly affected by the number of nodes in the network because of the logical record contention that's inherent in any complex multiuser file-access system.

In addition to the impact of the application, the exact hardware configuration can greatly impact the observed performance. The raw throughput of the LAN medium is important, but the

CPU speeds of individual nodes, the speeds of file server disks, the amount of cache memory, and other important factors all have an impact on the observed throughput in some way.

Benchmark Fallacies

Reported test values are often based on single-workstation (i.e., one file server, one workstation) configurations. While these values are reported correctly, you should not extrapolate the same performance levels across a multistation configuration. More representative performance figures can be derived from 6- to 10-workstation configurations, which is closer to the reported average number of nodes per network.

Too often, reported test results favor the evaluation of a single component of the LAN (e.g., a network card or file server) and do not reflect observable performance in a user application environment. The results from a READ/OVERLAY operation are typical of these types of tests. In this case, a single user file is cached at the server (and partially cached at the workstation), and the same data block is repeatedly read in a timed test. While this test may give some indication of the efficiency of the network interface card and driver, it doesn't reflect the I/O pattern of any known application.

In addition, many tests use 4096 bytes as a standard I/O size. This model does not fit most PC applications and gives results that are difficult to correlate to user applications. Tests modeled closer to a user application give more realistic results.

The best performance tool for any LAN evaluation is utilization of the target application itself. Only with this application can you accurately model the performance of the LAN. While any performance values generated by using this tool will be accurate, multistation tests are difficult to simulate because of the lack of a mechanism to automate and synchronize the stations.

Understanding all the factors involved in performance numbers is important in making a valid decision on your best network configuration. When choosing a LAN, be sure to consider how closely any reported tests reflect your application environment. Don't follow the numbers blindly.

passing work fine in a typical office environment, token passing is superior for process control applications that require real-time control over data delivery.

Hard Numbers

Quantifying the performance of a network is difficult because there is no accepted standard for determining LAN performance metrics. In lieu of a standard, I used common utilities to determine simple performance metrics for ARCnet, Ethernet, and Token Ring. The tests used simple DOS utilities on identical equipment to obtain a baseline performance metric for each technology. This provided a mean performance determination that normalized the effects of disk speed, workstation CPU speed, and server caching features. In all cases, I installed Tiara network adapters on a LAN using Novell's NetWare 2.12.

The first test copied the entire server disk across the network to the source station and determined the average K-bytes-per-second throughput. The second test used Novell's PERFORM2. Table 2 lists the results of the tests.

Observed performance in a LAN results from the complex interaction of many subcomponents within the LAN configuration. In evaluating complete systems, you should use tests that assess the impact of subcomponents such as network interface cards, workstation memory configurations, and CPU speed. See the text box "LAN Yardsticks" at left for more on evaluation.

Standards Issues

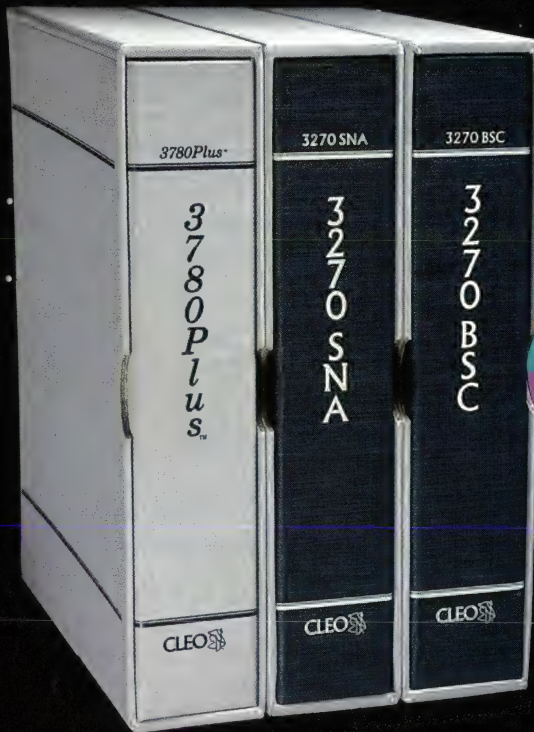
Standards have become more important as the LAN industry has matured. Fortunately, ARCnet, Ethernet, and Token Ring are all defined by a controlling body or standard that states exactly how the technology should be implemented.

Ethernet and Token Ring are defined by IEEE 802 (LAN technologies) committees. Specifically, the Ethernet protocol falls under the auspices of the 802.3 (CSMA/CD) committee, and Token Ring is controlled by the 802.5 committee. These committees have generated design specifications for their respective technologies; any product claiming to support one of these connection types must adhere to these specifications.

ARCnet is different: Datapoint acts as the controlling body for any implementation of ARCnet. Datapoint has final approval over all hardware implementations of the ARCnet technology to the point of being responsible for the microcode of all new ARCnet communication

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Table 2: The network consisted of a Compaq Deskpro 386/20 server, three 12-MHz 80286 workstations, two 10-MHz 80286 workstations, and one 8-MHz 80286 workstation. As expected, ARCnet trailed Ethernet and Token Ring in performance. Ethernet's superior showing probably reflects the configuration of the LAN rather than any inherent superiority over Token Ring.

LAN TESTING RESULTS

Connection type	Server-to-station	PERFORM2
ARCnet	200K bytes/second	137K bytes/second
Ethernet	450K bytes/second	971K bytes/second
Token Ring (4 megabits/second)	230K bytes/second	192K bytes/second

Note: 16 megabits/second not available.

controllers. Thus, ARCnet has remained "pure" even though it is not controlled by any governing standards body.

Best Choice?

There is no "best" LAN configuration per se. You have to weigh the importance of cost, performance, and functionality in configuring your installation. Each connection type has its good and bad points.

If cost is a driving concern for your LAN configuration, ARCnet is a good choice. No other LAN connection interface offers a "standard" product for such a low cost per node. ARCnet is simple to install and features very acceptable performance, especially in a typical office environment that on average contains fewer than 20 nodes.

If performance is a major concern, you should consider Ethernet. Because of

its CSMA/CD architecture, some people question Ethernet's ability to deliver high performance under a heavy work load. In all practicality, however, Ethernet performs very well in most situations. Ethernet costs more than an ARCnet installation, but the speed and connectivity features offset the higher price.

Token Ring provides good performance connections plus features such as simple connectivity to mainframe systems, simplified bridging for large networks, and more sophisticated protocol-tuning mechanisms. For full-featured networks, Token Ring is the technology of choice.

ARCnet, Ethernet, and Token Ring thrive in today's marketplace because each satisfies the requirements of certain customers. As long as you know your requirements, you will be able to select the connection option that's best for you. ■

Richard Watson is vice president of engineering/development for Tiara Computer Systems of Mountain View, California, which produces hardware and software products for LANs. He can be reached on BIX c/o "editors."

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THE LANGUAGE OF LASERS

PostScript and PCL establish a range of page-description languages while newcomer CaPSL fills in the middle

Kent Quirk

W

hen Hewlett-Packard introduced its printer-control language (PCL) level 1 with its first LaserJet printer, the company established the first standard for page-description languages (PDLs). But even after three revisions, PCL level 4 is an aging standard, challenged by two notable alternatives: Canon's newcomer CaPSL and Adobe's sophisticated PostScript.

The good news for laser-printer users is that each technology performs its job differently as a high-level printer language. Clear choices exist in a market where performance strides are a tradition (see the text box "Rigid Grids Spawned Today's PDLs" on page 206).

HP's PCL level 4

PCL level 4 can place black text at any location on a page, and page elements can be drawn in any order. Layouts begin at the upper left corner of the page, but application software isn't forced to create a page from top to bottom. For example, a program could draw a black border before the text is actually printed (see table 1a).

But PCL offers only bit-mapped fonts that cannot be scaled or rotated (although landscape fonts are available). PCL can't execute drawing commands more complicated than horizontal and vertical lines, which it implements as filled rectangles. It supports a few levels of gray (but not continuous shading) and several pattern fills for rectangular areas.

You begin nearly all PCL commands

by typing ESC followed by a punctuation mark and a letter. Numeric parameters and a terminating letter may follow. PCL considers any other character printable text.

PCL prints raster images using pixel replication to change resolutions. It supports macros and overlays to create frequently used logos and forms.

Complicated images must be handled by the CPU, which will generate a bit map and then print the figure. However, using the CPU for rasterization means larger code sizes, longer image transmission times, and a waste of CPU resources. For example, to print text at an odd angle, you must choose a host-resident font, draw the font into a bit map, and transmit the entire bit map as an image.

Canon's CaPSL

CaPSL, released last June, draws any shade of gray, places fonts in any orientation, and offers a selection of plotting commands for vector drawing. The language is designed to quickly transmit and execute page descriptions.

CaPSL implements a set of the ANSI/ISO screen control

continued



commands like those used by the AN-SI.SYS device driver and many computer terminals.

The command format is simple: Most sequences begin with the command sequence initiator (CSI), which consists of the Escape character followed by a left square bracket. (CaPSL also provides a single-character replacement for the CSI.) Following the CSI are parameter numbers separated by semicolons. The last parameter is followed by an intermediate character and a terminator, which together define the function to be executed. CaPSL considers anything not part of a command sequence to be printable text (see table 1b).

For example, CSI 10;20f instructs the printer to begin drawing at row 10, column 20 (f is the terminator). These command sequences are fast to transmit and interpret. They are also extensible while remaining within the standard. Unfortunately, they are difficult to read and program (but this shouldn't hinder most users).

Page layouts originate at the upper left corner. The y-axis is inverted from the normal Cartesian plane. Coordinate measurement is flexible. Positions can be specified in several coordinate systems. There are horizontal and vertical motion indexes, the size of which can be set according to each font. Position settings can be units measured in decipoints, mils, hundredths of millimeters, or device dots (1/300 of an inch).

CaPSL's high-level drawing commands include instructions for lines, polylines, rectangles, arcs, circles, ellipses, quarter-ellipses, and graphics markers for line graphs. CaPSL can't combine lines and arcs into a single fillable object, nor can it produce nonelliptical curves, such as Bezier curves. Although restricted to rectangles, clipping can make them precise to the nearest pixel, character, or string.

The language can handle both bit-mapped and scalable fonts, including outline-font "hints" that tell the printer how to draw a font in a different size. CaPSL uses hinted fonts internally. Its bit-mapped images can be downloaded as either binary or hexadecimal data. It can scale these images up through pixel replication by a factor of 1, 2, 3, or 4. Scalable-font characters can be scaled, rotated, skewed, outlined, shadowed, or filled with a pattern.

Macros include some programming-language features. Macros can execute other macros, or you can set a macro to run a specified number of times without conditionals or variables. This is helpful

Table 1: The following code samples (a) from HP's PCL level 4, (b) Canon's CaPSL, and (c) Adobe's PostScript each produce text in two different fonts and create a gray box bordered by 0.1-inch rules.

DECODING THREE PDLs

(a) PCL level 4

Command	Action
{ESC}E	Reset.
{ESC}(s0T	Select line printer.
{ESC}(s16.66H	Select 16.66 pitch.
{ESC}&a720v720H	Move to 1 inch (720 decipoints) from top and left.
This was generated in HP's PCL using the line-printer font at 16.66 cpi.	
{ESC}(s3T	Select Courier.
{ESC}(s10H	Select 10 pitch.
{ESC}(s3B	Select bold.
{ESC}&a1440v720H	Move to 2 inches from top, 1 inch from left.
This text is written in Courier Bold at 10 cpi.	
{ESC}*p1200x1200Y	Move to 4 inches from top and left.
{ESC}*c45G	Set 45 percent gray scale (HP doesn't have a 50 percent gray).
{ESC}*c300a300B	Box of 1 inch by 1 inch.
{ESC}*c2P	Print the gray box.
{ESC}*p1185x1185Y	Move to corner less width of line.
{ESC}*c330a30B	Box 1 inch by 0.1 inch.
{ESC}*c0P	Print a black solid rule.
{ESC}*c30a300B	Box 0.1 inch by 1 inch.
{ESC}*c0P	Print a black solid rule.
{ESC}*p1185x1485Y	Move to corner less width of line.
{ESC}*c330a30B	Box 1 inch by 0.1 inch.
{ESC}*c0P	Print a black solid rule.
{ESC}*p1485x1185Y	Move to corner less width of line.
{ESC}*c30a330B	Box 1 inch by 0.1 inch.
{ESC}*c0P	Print a black solid rule and print the page.

(b) CaPSL

Command	Action
{ESC}<	Soft reset.
{ESC}[2&z	Paint memory mode full.
{ESC}[?32h	Enable scaling character sets.
{ESC}[?33h	Enable character set rotation.
{ESC}[0p	Select page format.
{ESC}[2l	Units are 1/720 of an inch (decipoints).
{ESC}[11h	Set positional units to size.
{ESC}PzSwiss.ISO_USA{ESC}\	Select character set.
{ESC}[100 C	Set 10 point.
{ESC}[720;720f	Position to 1, 1.
This was generated in Canon's CaPSL using the Swiss font at 10 point.	

continued

in creating forms and logos. (Canon printers come with many preloaded macros that set up the printer to various modes or generate commonly used forms.)

Adobe's PostScript

PostScript can do things no other printer language can do. It offers an elegant and highly extensible approach to page gen-

eration, especially when an algorithmic specification is the only compact way to describe an image. But what PostScript offers in sophistication, it sacrifices in speed—PostScript generally is the slowest of the PDLs.

PostScript constitutes a complete programming language with features specific to generating printed images. Most printers accept printable text and embed

THE LANGUAGE OF LASERS

```
{ESC}PzDutch-Italic.ISO_USA{ESC}\
{ESC}[240 C
{ESC}[1440;720f
This is written
in 24-point Dutch Italic.
{ESC}[2880;2880f
{ESC}[0&}
#{|S2}
!0!1{|S2}
${|S2}
E101{|S2}
F1D8{|S2}
I(1{|S2}
};Bt0Ca0Bt0Ca0{|S2}
%{|S2}
}p{|S2}

Select alternate character set.
Set 24 point.
Position to 2,2.

Position to 4,4.
Change to virtual device metafile mode
with current origin.
Begin picture.
Set scaling mode (1/72 of an inch like before).
Begin picture body.
Set line type to solid.
Set line width to 72/720ths of an inch.
Set interior style (draw border, fill with gray).
Draw rectangle.
End picture.
End VDM mode.
```

(c) PostScript**Command**

```
/inch { 72 mul } def
1 inch 10 inch moveto
/Helvetica findfont
10 scalefont
setfont
```

(This was generated with PostScript in the Helvetica font at 10 point.)

```
1 inch 9 inch moveto
/Times-Italic findfont
24 scalefont
setfont
```

(This is written in 24-point Times Roman Italic.)

```
4 inch 7 inch moveto
1 inch 0 rlineto
0-1 inch rlineto
- 1 inch 0 rlineto
closepath
gsave
.5 setgray
fill
grestore
0.1 inch setlinewidth
stroke
showpage
```

Action

Define an inch for easy positioning.
Position to 1 inch from top (10 inches from bottom).
Get the font.
Scale it to 10 point and tell PostScript to use it.

Draw the next text.
Change to Times Roman Italic.
24 point.

Draw the box.

We've defined the box as a closed path.
Remember the path.
Use 50 percent gray and fill it.
Get the path back.
Use fat lines and draw the outline.
Print the page.

the specially coded commands in the data stream. But PostScript reads its data stream as a set of commands, so you must enclose text in parentheses for it to print. A PostScript page description is really a program, and the text it generates is just a set of strings within that program (see table 1c).

As a programming language, PostScript is designed to be read and exe-

cuted in one pass, without backing up. A PostScript program usually is machine generated, although it is based on a set of English keywords.

The result is a language similar to but more readable than Forth. PostScript offers a stack-oriented architecture, with separate dictionaries to hold data and code for random access.

continued

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Rigid Grids Spawned Today's PDLs

In the past 10 years, printer manufacturers have steadily developed more-sophisticated ways to put marks on paper. As printer technology evolved, many people changed their ideas about what actually is a printer.

In the mid-1970s, people saw printers merely as a means for putting text on paper. The output page was an imaginary grid, and a printer placed vertical letters into boxes within the grid. Letters were a fixed size and shape, and they generally came from fully formed characters. You could print pages quickly or print them to look good, but trying to do both required expensive equipment. In any case, bold-facing was about the only choice for emphasizing text, and you accomplished this by changing the daisy wheel or overprinting. Languages used to control printers were simplistic. A few control characters moved the printer carriage left, right, up, and down.

The Diablo 630 daisy-wheel printer defined a control-language standard. Even today, most word processors and many printers support this minimal control language. The most expensive printers used proportional type for a "typeset" look, but few word processors took advantage of it.

The dot-matrix printer evolved as an inexpensive way to produce characters quickly. Initially, dot-matrix printers were considered to have poor quality. As recently as the mid-1980s, business

correspondence relied on daisy-wheel printers, despite the heavier weight, louder noise, and slower speed.

But dot-matrix printers offered more flexibility. They provided a choice of two or three different (if ugly) fonts and two or three sizes of text. You could add emphasis to words without babysitting the printer. Text was still defined as letters in boxes, but now you could vary box sizes and create proportionally spaced text.

As ROM and microprocessor prices dropped, dot-matrix printers grew more intelligent. Old, one-character control sequences became two and three characters long, but they were generally invented from whole cloth by the manufacturers. A minimal standard of Epson compatibility arrived to keep the peace, but most manufacturers added to it in little (or not so little) ways.

The dot-matrix printer defined a smaller grid on the page, and you could fill any grid location with a dot or leave it blank. This meant that PCs could draw graphs or characters of arbitrary shapes and sizes. Unfortunately, pages had to be generated from top to bottom, which strained memory and computing power. Also, the process was slow, taking minutes per page. Resolution was poor, typically 72 dots per inch. Worst of all, some companies that claimed Epson compatibility apparently never tested their printers with an appropriate program.

Fonts lacked standardization. It was obvious that most programmers and printer manufacturers created their own fonts. Vendors found thousands of ways to make the letter *A*, and most of the letters looked bad. Even when individual letters were not hideous, they often looked unrelated to other characters within the same font.

Later, laser printers and 24-pin dot-matrix printers became affordable. They offered vastly improved resolution, greater intelligence for better graphics, and enough resolution to print recognizable fonts. Initially, manufacturers packaged standard fixed-width typewriter faces, such as Courier and Prestige, in proportional and nonproportional forms. Some vendors sold downloadable fonts or font cartridges, which provided a variety of fonts at full printer speed. Programs using the graphics mode to generate interesting pages became available.

Note, however, that printers still divided printing "text" (now defined as horizontally oriented letters in a predefined font collection) from printing "graphics" (which are simply patterns of bits). The printing program was still bound by the printer's mechanical characteristics, such as resolution, available fonts, and size of font characters.

Today, with the advent of page-description languages (PDLs), a printer's task is evolving further into the job of placing marks on a gridless page.

PostScript's biggest (and for some, debilitating) problem is that it is slow. Optimization techniques and interpreter aids help, but in general, an image produced by PostScript takes longer than creating the same image in another language. Also, most PostScript printers use a serial interface, so even simple images can reach a bottleneck when you try to send them to the printer.

Imaging Model

The PostScript imaging model is important. PostScript draws with various colors of paint on paper, and the paint is opaque. For monochrome printers, the paint varies from white through shades of gray to black. For color printers, you choose the color as relative levels of red, green, and blue, or as hue, saturation, and brightness, depending on your needs.

Drawing commands include arcs, lines, and Bézier curves. Drawings consist of a path, which is a set of connected or disconnected lines and curves. A path can be stroked (i.e., traced with paint). Closed paths can be filled (using either of two fills), used as a clipping boundary, smoothed, converted to line segments, or processed in various ways.

PostScript isn't dependent on the output device's resolution until it draws into the bit map with the show, stroke, or fill operators. Elements are then converted into pixels at the device's resolution.

PostScript's measurement system is device independent. The default unit is the printer's point (1/72 of an inch), and the coordinate system is arranged in Cartesian form, with the origin at the lower left corner of the page. With a few exceptions, points are first processed through

a translation matrix that lets the programmer use any coordinate system with two axes on a plane. You can directly manipulate this matrix or use scale, translation, and rotation operators.

PostScript typically stores fonts as outlines and then converts them to bit maps during printing. A printer font cache stores bit maps as they are generated, greatly improving text-processing speed with reused characters. PostScript fonts also function as paths, so you can treat letter forms as outlines for special purposes.

Font outlines must change with the device resolution and point size. Adobe fonts resident in PostScript include hints that tell the printer how to render outlines for different type sizes. Adobe won't reveal how to do this, although it

continued

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Inquiry 912.

PostScript

Adobe Systems, Inc.
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P.O. Box 7900
Mountain View, CA 94039
(415) 961-4400
Inquiry 913.

ter than a downloaded version of the same font.

Bit-mapped images plague PostScript, even though it can scale them into arbitrary sizes. Because its input data stream cannot handle binary data, this data is often sent in hexadecimal form, doubling the image size and the transmission time.

Given PostScript's abilities, why doesn't everyone just go out and buy it? Its lack of speed can be impractical, especially for systems that generate hundreds of pages a day, such as print servers on large LANs. Unlike PostScript, CaPSL features speed optimizations like marker drawing commands and image compression. A normal PostScript page description as generated by current word processing programs is significantly longer than the same page as described by CaPSL or PCL. PostScript can't cope with something as simple as a PrintScreen key press, because it can't handle straight text. Finally, PostScript is expensive. Until the recent PostScript clones hit the market, PostScript added \$1000 to \$2000 to a printer's cost.

Products such as Custom Applica-

tions' Freedom of the Press and Laser-Go's GoScript now implement PostScript in software on the host computer and then send a bit map to a printer in raster-image mode. This approach is also slow, but it may be an alternative at sites where PostScript is used only occasionally.

A vast array of software products supports PCL, so it's a safe purchase for those wanting laser-printer resolution. With newcomer CaPSL, Canon is betting that a market segment needs more functionality than PCL but not as much as PostScript's. Even if CaPSL becomes a contender, powerful PostScript will likely remain the technology of choice for typesetting and image processing. However, as laser-printer processing improves, the speed and price gaps between PostScript and its competitors will probably continue to shrink. ■

Kent Quirk is a freelance writer and president of Totel Systems, Inc., in Westford, Massachusetts, a company that develops device drivers and embedded software. He can be reached on BIX as "kquirk."

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A STANDARDS DICTIONARY

Which IBM PC standards have stood the test of time and are working well for vendors and users? Here are a few that fill the bill.

L. Brett Glass

The IBM PC architecture has spawned literally hundreds of standards, conventions, and common practices throughout the industry. At this point, seven years after the introduction of the PC, it's worthwhile to take a good look at this collection of standards and see how far we've come and, by extrapolation, where we're going.

The following list is limited to PC- or IBM-specific standards (SCSI, for example, does not qualify because it can be used with virtually any machine). And while this list has numerous entries, it is by no means complete. (Terms in italics are discussed under their own headings.)

.ARC File Format

This is the file format used by the ARC file-compression program, published by System Enhancement Associates (SEA) of Wayne, New Jersey. Programs from several other vendors read and write files in this format—most notably, PKARC and PKPAK utilities from PKWare, which added to the standard by providing additional compression options. (Although still available on many BBSes, PKARC

and PKPAK have been discontinued due to litigation by SEA.) Neither the original ARC program nor the file format is PC-specific, but the program gained most of its popularity and installed base in the PC marketplace.

.DBF File Format

This is the file format used by Ashton-Tate's dBASE programs. Products from

many vendors other than Ashton-Tate read and write this format.

.PCX File Format

This is the file format for images produced by ZSoft's PC Paintbrush (ZSoft is in Marietta, GA). It's a common graphics file format on the PC and is also used by most scanners, fax programs, and desktop publishing programs.

.ZIP File Format

The file format for PKWare's PKZIP utility, this is a compression and archiving program similar to SEA's ARC.

8514/A Graphics Adapter

This is IBM's current top-of-the-line graphics adapter. It can display 1024 by 768 pixels in as many as 256 simultaneous colors. A number of third-party intelligent graphics adapters emulate the 8514/A as well as providing their own sets of graphics commands.


Advanced Basic Input/Output System (ABIOS)

The ABIOS is a set of low-level routines that is similar to the PC's real-mode BIOS, but the ABIOS is designed to work in protected mode. It

continued



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EXPANDED MEMORY SPECIFICATION (EMS)

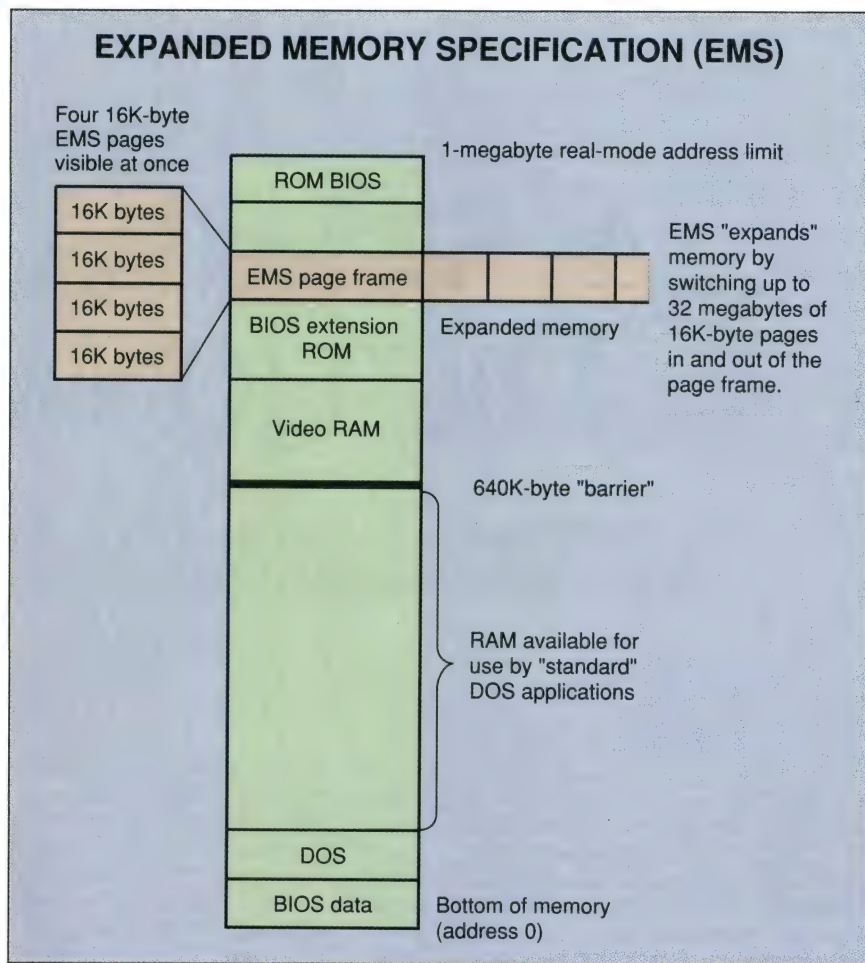


Figure 1: To remember the difference between EMS memory and extended memory, you can think of the bank-switching process as "expanding" the memory map laterally rather than vertically.

comes standard on every PS/2 machine, but it is not present on IBM's older machines or on most clones. (See "The IBM PC BIOS," April BYTE, for a comprehensive description of the A BIOS and how it works.)

Advanced Program-to-Program Communication (APPC)

The APPC is the part of IBM's System Network Architecture (SNA) that allows processes on the same or different machines to communicate with one another. APPC is designed to be implemented on a wide variety of hardware. It is sometimes called LU 6.2; in fact, the two are intimately connected but are not the same thing. APPC refers to the higher layers of the protocol and its application program interface (API), while LU 6.2 refers to the software that implements APPC on a given machine. (For more on this protocol, see "A Logical Choice," January BYTE.)

Basic Input/Output System (BIOS)

The BIOS is the heart of the PC and is among the most important factors in PC compatibility. (For a comprehensive discussion, see "The IBM PC BIOS," April BYTE.)

Color Graphics Adapter (CGA)

The CGA was one of the first two display boards offered for the IBM PC (the other was the *monochrome display/printer adapter (MDA)*). The CGA has a maximum graphics resolution of 640 by 200 pixels (two colors only) and can display, at most, 80 columns by 25 lines of text. All later IBM offerings are capable of emulating the CGA on a color screen.

Communicating Applications Specification (CAS)

CAS is an API that allows programs to communicate with Intel's Connection CoProcessor fax modem card. (See "Making Applications Talk," January

BYTE, for further information on this standard.)

Enhanced Industry Standard Architecture (EISA)

EISA is a bus that theoretically will be upwardly compatible from the *industry standard architecture (ISA)* and offer enhanced performance. EISA's development currently is being finalized by a consortium of compatible vendors. Some 200 vendors have paid for the details of the specification. EISA was designed to compete with IBM's *Micro Channel architecture (MCA)*. Intel recently finished development of an EISA chip set.

Enhanced Expanded Memory Specification (EEMS)

EEMS was proposed by AST Research as an extension to the original Lotus/Intel/Microsoft *EMS*. EEMS allows more than one 64K-byte area of RAM to be paged in and out at a time and lets applications run from the bank-switched RAM. Both these features were incorporated into version 4.0 of EMS.

Enhanced Graphics Adapter (EGA)

The EGA, IBM's enhanced follow-on to the *MDA* and *CGA*, incorporates all the text and graphics modes of both—plus a few more. It can produce a high-resolution monochrome display similar to that of the *Hercules graphics card (HGC)*. Unlike the HGC, though, the EGA can display graphical pixels in two intensities and has different numbers of pixels in each row and column.

In its color modes, the EGA can produce an output signal equivalent to that of the *CGA* or a denser, higher-quality color image with a greater scan rate. (The standard EGA monitor switches between these two rates.) The EGA has a software-selectable color palette and limited pixel-manipulation hardware on-board. Despite the introduction of the more powerful *professional graphics adapter (PGA)*, the EGA remained the dominant color graphics standard for the PC until the *multicolor graphics array (MCGA)* and *video graphics array (VGA)* were introduced.

Expanded Memory Specification (EMS)

The Expanded Memory Specification allows access to more than 1 megabyte of memory on a standard IBM PC by bank-switching 16K-byte blocks of RAM in and out of one or more 64K-byte areas called page frames (see figure 1). Versions of EMS before 4.0 allowed only one page frame with four 16K-byte pages

to be visible at any one time; 4.0 extended the standard to allow any portion of RAM to be switched in this manner. This and other features of EMS 4.0 were adapted from AST Research's *EEMS*.

Extended Memory Specification (XMS)

The XMS manages extended memory on AT-class and 80386-based PCs. Before XMS, there were only ad hoc standards for reserving parts of this space; even IBM's *VDISK* and disk caching programs used different techniques.

XMS defines an API that allows you to reserve blocks of extended memory (extended memory blocks, or EMBs) and transfer data between them and the lowest 1 megabyte of RAM (i.e., the area available to real-mode programs). Figure 2 shows how XMS can also give real-mode programs access to almost 64K bytes of additional memory in an area that is known as the high memory area (HMA).

The area from hexadecimal addresses FFFF:0010 to FFFF:FFFF can be addressed from real mode if the A20 line of the CPU is enabled; an XMS driver can reserve that area of memory for a program and take charge of enabling and disabling A20.

Finally, XMS manages blocks of memory between 640K bytes and 1 megabyte in the processor's "normal" address space. Add-on cards sometimes provide chunks of RAM that fall into this area; XMS allocates the space as upper memory blocks.

Graphical Environment Manager (GEM)

A graphical windowing environment created by Digital Research (Monterey, CA), GEM runs not only on PCs but also on Atari STs. Many applications, including Xerox's *Ventura Publisher*, run in the GEM environment.

Grafrax

Grafrax is actually Epson's standard for performing graphics on a dot-matrix printer. But IBM's decision to use Epson as the OEM for the IBM Graphics Printer meant that Grafrax became a de facto standard for IBM PC graphics output. Most laser printers for the PC can emulate an Epson printer running Grafrax.

GW BASIC

Because of the large number of features this language contains, the "GW" in the name of Microsoft's *GW BASIC* reputedly stands for "Gee Whiz." Derived

continued

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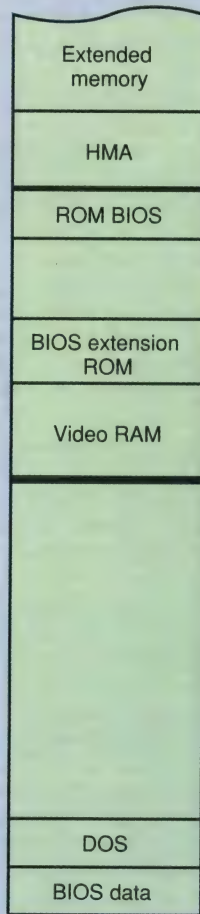
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EXTENDED MEMORY SPECIFICATION (XMS)



Extended memory above high memory area (HMA) is allocated as extended memory blocks and cannot be accessed directly from real mode.

The HMA is the first 65,520 bytes above 1 megabyte. You can access this area in real mode by doing tricks on an AT or compatible. 1-megabyte real-mode address limit.

Any unused space in this area can be filled with RAM and allocated as upper memory blocks. XMS will not interfere with EMS.

640K-byte "barrier"

RAM available for use by "standard" DOS applications

Figure 2: Extended memory is the area above the 1-megabyte mark on an 80286- or 80386-based PC; it's simply a linear extension of the RAM below 1 megabyte.

from Microsoft's CP/M BASIC, GWBASIC has been largely supplanted by newer offerings such as QuickBASIC and Turbo BASIC. Nevertheless, GWBASIC is still an important standard in the PC world because IBM shipped it with all its machines.

Hercules Graphics Card (HGC)

Of the original IBM PC display adapters, neither the CGA nor the MDA provided everything early PC users wanted. The CGA could display graphics but used a coarse 8- by 8-character cell; the MDA displayed much clearer 9 by 14 characters but could show only text.

The Hercules graphics card, introduced during the early days of the PC, gave users the best of both worlds (except for color). It emulated the MDA and ran on the same monochrome TTL display, but it added monochrome graphics capabilities with a higher resolution than the

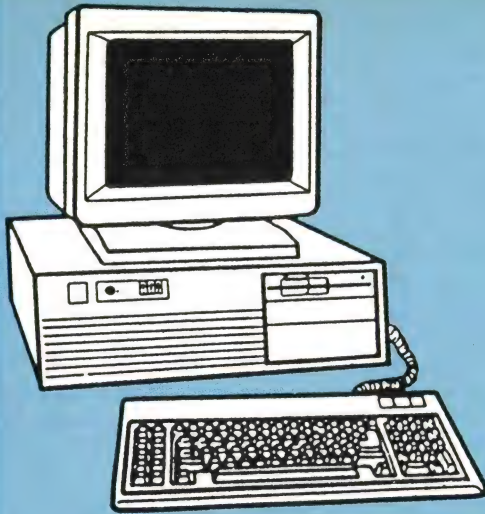
CGA's. It also included a parallel printer port like the MDA's.

Generally speaking, the HGC has now been outmoded by newer adapters that bring the same resolution (or better) to color screens, but it remains one of the most successful third-party graphics board standards.

Industry Standard Architecture (ISA)

ISA refers to the bus signals and timings used in the original PC and AT computers. Because no formal timing specifications have ever been published for this bus, it has been thought of as an ad hoc standard; to this day, peripheral cards are often tested empirically for ISA compatibility. Proponents of EISA and MCA believe that one of these newer architectures will eventually replace or supersede ISA.

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	Mono	EGA	VGA
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20MB	1190	1640	1715
40MB	1345	1795	1865

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- Enhanced 101 key keyboard
- AT full style case
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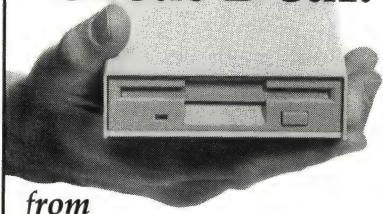
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Micro Channel Architecture (MCA)

With the advent of the PS/2 machines, IBM introduced the Micro Channel architecture, a multimaster, fully specified 16-/32-bit bus with a minimum cycle time of 100 nanoseconds. The MCA is IBM's contender to replace *ISA*, but it is seeing only a limited acceptance due to incompatibility with existing cards and IBM royalty considerations.

Microsoft Windows

Microsoft Windows (and its 80286 and 80386 cousins) is a windowing and multitasking environment for PCs and compatibles running *MS-DOS* or *PC-DOS*. The Windows user interface resembles that of IBM and Microsoft's *Presentation Manager* for *OS/2*.

Monochrome Display/Printer Adapter (MDA)

MDA was one of the original display options on the PC. Driving a high-persistence TTL monochrome monitor with two display intensities, the MDA showed 25 lines of 80 characters each. The 9- by 14-character cell made this adapter superior to the *CGA* (which used an 8- by 8-character cell) for text.

Microsoft Disk Operating System (MS-DOS)

This PC operating system had its origins in an 8086-based CP/M clone, 86-DOS, created by Seattle Computer Products.

MS-Net

MS-Net is Microsoft's standard for networking *MS-DOS*. Using a redirector and *NetBIOS*, an MS-Net-based network allows peer-to-peer networking through the *server message block (SMB)* protocol.

Multicolor Graphics Array (MCGA)

IBM introduced the MCGA as part of the PS/2 Model 30. It provides some of the capabilities of IBM's *VGA* display adapter and runs with a PS/2 analog monitor.

NetBIOS

NetBIOS is an API that lets programs running on IBM PCs access a LAN. Commands are provided to control activity on the Medium Access Control and session layers of the International Standards Organization protocol stack; all other layers are hidden. *MS-Net* uses NetBIOS to implement peripheral sharing. (See "Understanding NetBIOS," January BYTE.)

OS/2

OS/2 is a protected-mode multitasking operating system developed by IBM and

Microsoft for the AT, PS/2s, and other machines with Intel 80286, 80386, or 80486 microprocessors. Although it is not in widespread use at the present moment, *OS/2* (along with *Presentation Manager*, its graphical user interface) is slowly gaining popularity in the PC marketplace.

PC-DOS

IBM's PC-DOS is an OEM version of *MS-DOS*. There are various versions of PC-DOS that populate the majority of PCs and compatibles.

PC-DOS-CP/M Text File Format

The text file format used by *PC-DOS* is the same as that used by its ancestor, CP/M. Lines are terminated by both a carriage return character (CR, ASCII code 13) and a linefeed character (LF, ASCII code 10), and the end of the file is indicated by a Control-Z. (Many PC-DOS programs omit the latter convention and rely on the operating system's record of the file size.)

Although this file format doesn't have an official name, all files sent as text via the XMODEM protocol, for instance, must be converted to it before being transmitted. Other operating systems (such as Unix) use a linefeed character alone to end a line; still others use a lone carriage return.

Presentation Manager (PM)

Presentation Manager is the graphical user interface standard developed for *OS/2* by IBM and Microsoft. (It was first shipped with *OS/2* 1.1.) PM uses overlapping windows, each containing an optional mouse-driven menu. PM is an evolving standard; one of the most significant ways that *OS/2* 1.2 is expected to be different from 1.1 is in its greater use of icons.

Professional Graphics Adapter (PGA)

The IBM professional graphics adapter was a high-end intelligent graphics board mostly used for CAD applications. Due to several factors, PGA did not become a popular standard.

RS-232 Connector (nine-pin)

When IBM decided to make a combination serial/parallel adapter for the AT, a small connector format was needed to allow both of the interfaces to fit on the back of a standard *ISA* interface card. Because the parallel connector could not be shrunk, the serial connector was; subsequently, the nine-conductor pin-out for

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RS-232C became a de facto industry standard. The nine pins are assigned as follows:

- 1—carrier detect; 2—receive data; 3—transmit data; 4—data terminal ready; 5—ground; 6—data set ready; 7—request to send; 8—clear to send; 9—ring indicator.

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TesSerRact (TSR)

TesSerRact is a standard developed by a team of programmers on CompuServe for terminate-and-stay-resident programs for the PC. TSR programs developed to this standard can coexist amicably with one another and can be removed safely from memory. TesSerRact builds

on the work of an earlier standardization effort called Ringmaster.

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L. Brett Glass is a freelance programmer, author, and hardware designer residing in Palo Alto, California. He can be reached on BIX as "glass."

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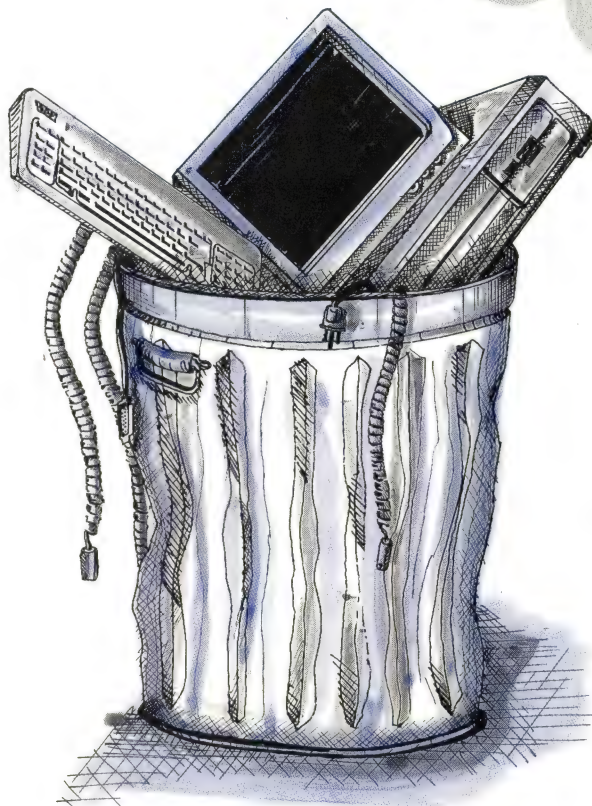
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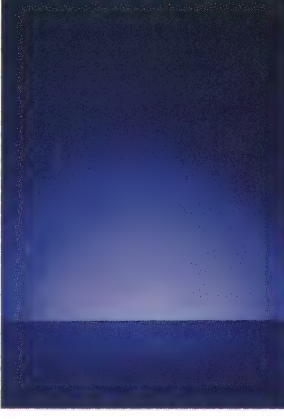
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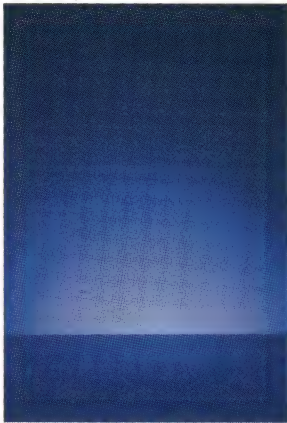




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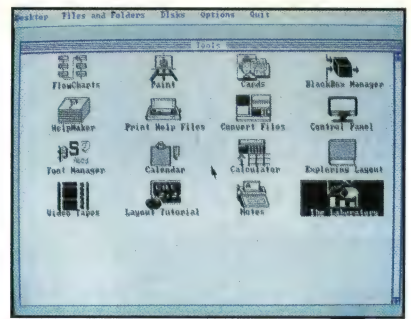
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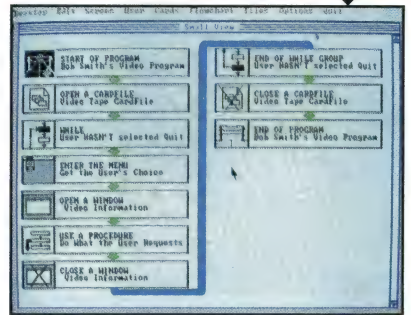
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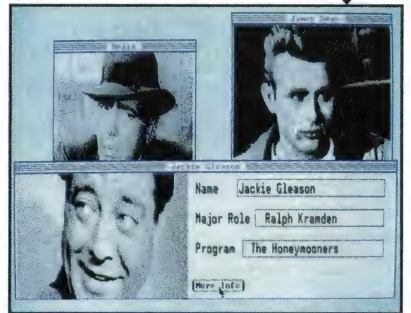
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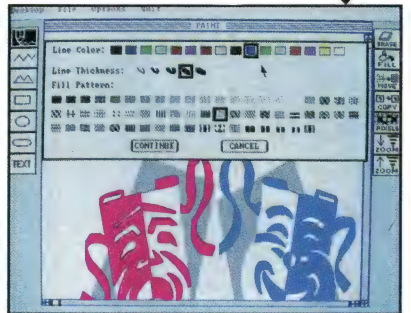
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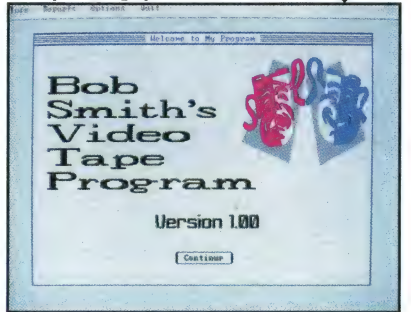
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OPTIMIZING NUMERIC COPROCESSING

*Advanced numeric devices need quality code
to deliver rated performance*

Stephen Fried

Until the day arrives when CPUs with on-chip FPU's, such as the 80484 and T800, perform floating-point operations in a single cycle, there will be a need for numeric coprocessors like the Weitek 3167 and 4167. These devices employ large areas of silicon to perform multiplication and addition nearly as fast as they are fed operands and operators. That also makes them exquisitely sensitive to the quality of the CPU code that drives them. I'll explore how compiler optimizations can yield a nearly sixfold increase in the speed of a Weitek 3167.

The art of generating fast-running programs boils down to two problems: transforming the program into a new program that is faster but gives the same results (optimization) and choosing the fastest sequence of processor instructions for that new program (code generation).

A compiler's *front end* includes components specific to a particular language: the scanner, which recognizes lexical elements, and the parser, which builds a tree-structured representation of the program. The compiler's *tree walker*, or intermediate

section, traverses the representation and rearranges it in a more efficient form. The *back end*, or code generator, writes the object code. You can find and perform optimizations in the front end and the intermediate section.

Front-End Optimizations

The most common front-end optimizations are strength reductions—transformations that replace one run-time calculation with another, faster one.

For example, the FORTRAN expression $(x**2)$ can be replaced by $(x*x)$; simple multiplication is about 10 times faster than exponentiation. For an 80386 running with a 3167, it pays to perform this strength reduction for integral exponents that fall between -4 and 11 .

Other opportunities for strength reduction are cases of multiplication or division by 1 or -1 ; multiplication, subtraction, or addition of 0 ; and addition or subtraction of 1 . However, the new generation of coprocessors invalidates some previously standard strength reductions. For example, it used to be faster to add or shift than to multiply, so an excellent reduction was to convert multiplications to a series of shifts and additions where possible. The more powerful multipliers of the latest generation of coprocessors render that optimization unnecessary.

Not all strength reductions are made in the interest of generating the best code. For example, many compilers perform the famous Whetstone strength reduction $\exp(\ln(u)) = u$. This reduc-

continued



tion—only one of a number of similar ones that could be made but are not—plays a key role in the speed of the Whetstone, which affects the sales of chips and compilers but little else.

The other common front-end optimization is the reduction of constant expressions into literal constants. If the compiler can determine that an expression's arguments are constants, it can perform the operation itself and replace the operator node in the tree with a constant node.

Intermediate Optimizations

Among the intermediate optimizations are eliminating code that never executes or whose output is never referenced, moving loop-invariant code outside loops, rearranging loops, caching (placing in registers) hot variables and addresses used in loops, and eliminating common subexpressions. Such optimizations are normally accompanied by a data-flow analysis that generates statistics about each block, procedure, and variable in the program. These statistics will be used downstream by the code generator. Since all this information is stored in the tree, the process is often referred to as "decorating the tree."

Intermediate optimizations can make a huge difference in the way some code performs and hardly any in other cases. Why? If you write code that already incorporates these optimizations, there's little the compiler can improve. In practice, though, manually optimized code isn't very legible, so many programmers prefer to write more readable code and let the optimizer spruce it up. Most programs do benefit from optimization.

Inlining of procedures is an important optimization. As more programmers write in C and use structured techniques, the overhead of function calls becomes significant. Such programs tend to jump around as much as they execute. Assume that it takes 100 cycles to call and return from a function that takes only 20 cycles to execute. Placing the procedure in-line (i.e., within the main program flow) yields a fivefold improvement.

The technique used to inline functions is to compile all the procedures in an application into unoptimized trees, taking statistics about each. Then the tree-walker decides whether to graft a procedure onto the tree (i.e., inline it) or call it. Inlining plays a crucial role in speeding up systems that incur a big penalty when required to refill the processor's pipeline.

Generating Code

Register allocation is the crucial issue here. The forthcoming generation of

Listing 1: FORTRAN code for the crucial section of the Whetmat benchmark.

```

INTEGER I,J,K
DIMENSION A(140,140),B(140,140),
           C(140,140)

DO 150 I = 1,100
  DO 140 J = 1,100
    C(I,J) = 0
    DO 130 K = 1,100
      C(I,J) = C(I,J) + A(I,K)*B(K,J)
    CONTINUE
  140 CONTINUE
150 CONTINUE

```

Listing 2: Pseudocode for the crucial section's inner loop.

```

start:
compute the address of the i,kth
element of A
load A(I,K) in fp register 1
compute the address of the k,jth
element of B
multiply B(K,J) with the contents
of fp register 1
compute the address of the i,jth
element of C
add C(I,J) to fp register 1
compute the address of the i,jth
element of C
store the contents of fp register 1
to C(I,J)
increment k
test k and jump to start if less
than 101

```

Listing 3: The inner loop with register-caching optimization.

```

DUM = 0
DO 130 K = 1,100
  DUM = DUM + A(I,K)*B(K,J)
130 CONTINUE

```

computers will be able to do 20 to 40 million floating-point operations per second (MFLOPS) as long as everything stays on-chip. Variables that stay in registers can be accessed much faster than those in the cache or off-chip memory. Going off-chip for operands is like throwing out an anchor from a sailboat—something you just don't want to do. Intelligent register allocation is the way to prevent that.

A good compiler analyzes variable usage over procedures before it allocates registers. It also tries to keep the number of variables that are register candidates as large as possible until the allocation has occurred. Even with data-flow analysis, this task is complicated by the possibility of aliases (i.e., multiple variables that refer to the same location). So the code generator tries to minimize the analysis by doing a very thorough job on

just the hot spots in the code. This compromise works well.

Peephole optimization smooths out the rough edges in machine-generated code. Its name reflects the small (two- or three-instruction) window, or peephole, used to examine the code. The peephole optimizer looks for short sequences that are easy to recognize and reduce. For example, the sequence

```

push  eax
pop   eax

```

is a meaningless piece of code that can be removed in the peephole stage.

Benefits of Optimization

Now I want to present two benchmarks I've adapted from the Whetstone benchmark. The first, which I call Whetscale, tests scalar floating-point arithmetic and measures raw coprocessor speed. This benchmark is available on BIX along with several other benchmarks under "jmicroway." The second, which I call Whetmat, does a matrix multiply, which complicates the arithmetic with indexing. In the Whetmat, the interaction between CPU and FPU makes good optimization especially critical. I'll trace what happens to the speed of the Weitek 3167 as the various optimization and code-generation features of a FORTRAN compiler are successively enabled.

When compiled with a globally optimizing compiler, the Whetscale measures the rate at which a numeric coprocessor performs elementary register-to-register floating-point operations. These operations are always the fastest because they don't reference memory and can take advantage of the wide internal data paths inside the coprocessor. The Whetscale code is an example of a piece of software that is 100 percent floating-point-bound and for which it is easy to figure out what the precise floating-point activities are: 12 additions, 1 negate, 4 multiplies, and 4 floating-point stores and loads. I developed a weighting scheme that produces a result measured in Whetscales, and these can be interpreted as the number of scalar floating-point operations per second. Since there are no 80386 instructions in the code, the Whetscale—when compiled optimally, with all variables in registers—places an upper limit on coprocessor speed.

I ran the Whetscale on several machines. The 25-MHz Acer was representative of the best results. With a 25-MHz Weitek 3167, the Acer achieved 3.05 MFLOPS. The 25-MHz 80387 result was, by contrast, .798 MFLOPS. The re-

sults can be interpreted simply. The Weitek 3167 does over 3 million basic floating-point operations per second, the 80387 only about 800,000. Used as a baseline, the Whetscale makes it possible to figure out how much time other benchmarks waste doing address calculations and fetching operands from memory. For example, I weighted the Whetmat in the same way I weighted the Whetscale but at best got only 1.7 MFLOPS from the 3167 (see next section). From this I concluded that an optimally coded 3167 vector operation spends 40 percent or more of its time performing nonnumerical activities.

The Whetmat Benchmark

I designed the Whetmat benchmark to measure the speed of a single-precision matrix multiplication. This is the kind of real-world problem at which a good FORTRAN compiler must excel. It also shows how optimization is the key to high-speed numeric processing. Listing 1 shows the most time-consuming part of the Whetmat. It's slowed by several things: two floating-point operations per iteration of the loop, address calculations for all elements in the arrays, and operand fetches from memory.

As I enabled the various optimizations of the NDP FORTRAN compiler, the results improved by a factor of 5.8. This actually means that as the code improved, the number of 80386 cycles required to support the Weitek 3167 declined by a factor of 5.8.

Listing 2 shows how a nonoptimizing compiler would handle the Whetmat's inner loop. You can see immediately that the address of C(I,J) is computed twice per iteration—a waste of time. There are three ways to tackle this problem. A compiler that can remove local common subexpressions would analyze this block, discover that the second address calculation was redundant, and eliminate it. Similarly, a compiler that can remove global common subexpressions would find that the address of C(I,J) was computed in the previous block (when the referenced element was initialized to zero) and use this address for both references since neither I nor J can change after the initialization. If the register allocator placed commonly used addresses in registers, this would result in slightly better code. Finally, since neither I nor J changes in the loop, they're loop-invariant (as are any expressions that depend solely on them) and can be taken out of the loop. Of these three methods, the first is usually available, the second sometimes, and the third rarely, because

it depends on data-flow analysis.

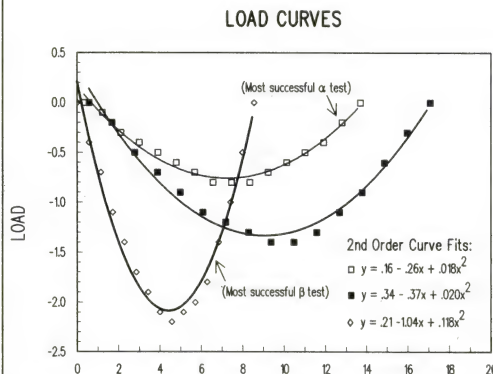
Once you've handled the redundant address calculation, though, you've barely scratched the surface. The computation of the addresses of the inner loop variables is the next candidate for simplification. These addresses depend on the single variable K and several constants that don't change (I, J, and the size of the array) as K does. K is an induction variable; the compiler figures out that, every time K increments, it's necessary to add

4 to the current address of A and $4 \times 140 = 560$ to the address of B. It accomplishes this by setting up registers to hold the addresses of A and B and incrementing them by 4 and 560 at the end of the loop. This optimization, in conjunction with the previous one, boosted performance on the Weitek from .29 MFLOPS to .77 MFLOPS.

Next, the compiler can take advantage of the fact that the array elements C(I,J)

continued

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refer to a single entity from the point of initialization to the end of the inner loop. This entity should be treated like a scalar for the course of the calculation. That way, the code generator can leave C(I,J) in a register for the duration of the inner loop, where it really belongs. The effect of this optimization is to transform the inner loop into the fragment shown in Listing 3. This transformation is called register caching. Few compilers perform it because in addition to a global data-flow analysis it requires a careful search for aliases. Because even some of the best mainframe compilers don't do register caching, well-written programs like LINPAK explicitly use dummy variables in place of array elements when the array element is being used as an accumulator. With register caching turned on, performance jumped to 1.11 MFLOPS.

At this point, you're starting to scrape the bottom of the barrel. The next optimization depends on an idiosyncrasy of the 80386 prefetch mechanism and works in conjunction with advanced 80386 addressing modes. The trick employed here, called loop unrolling, entails placing sets of four loop iterations

in-line. It takes more space but runs much faster because it keeps the processor's pipeline filled. Since the 80386 has to fill its prefetch queue every time it makes a jump, unrolling the loop yields considerable savings. At the same time, the compiler can use base addressing mode with an immediate constant that increases by 4 and 560 on each roll through the loop. Loop unrolling brought the benchmark result to 1.4 MFLOPS.

There's one more possibility. Because dot products are so important in the numerics repertoire, advanced FPU's like the Weitek 3167 often supply a special instruction to perform them. It's called the multiply/accumulate, and NDP FORTRAN supports it. With the multiply/accumulate switch turned on, the benchmark result jumped to 1.7 MFLOPS.

In the process of turning on these optimizations, Whetmat performance went from .291 MFLOPS to 1.7 MFLOPS—a nearly sixfold improvement in code quality. There's another way to look at this: The code in the inner loop of this program was reduced in size by a factor of almost 6. By counting the 80386 op codes executed per inner loop in each

case, I determined that the increase in speed over the whole range of the experiment was virtually identical to the reduction in the number of 80386 op codes per loop—that is,

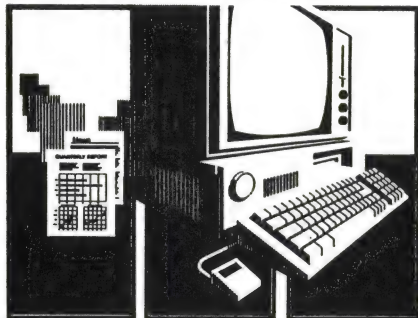
$$\begin{aligned} \text{ratio of throughput} &= 1.7/2.91 = 5.8 \\ \text{ratio of 80386 op codes/loop} &= 23/4 \\ &= 5.75 \end{aligned}$$

These results prove my thesis. In situations where numeric operations run as fast as basic CPU operations, the crucial issues in attaining rated numeric throughput are register allocation and reduction of the number of CPU operations required to support the numerics. The next generation of numeric processors will reach their full potential only with the help of advanced optimization techniques that minimize the number of supporting 80386 (or 80486) operations. ■

Stephen Fried is well known for his work in chemical lasers and the use of numeric coprocessors in the IBM PC. He is vice president of R & D at MicroWay, Inc., in Kingston, Massachusetts, and can be contacted on BIX c/o "editors."

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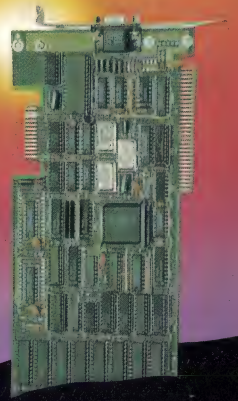
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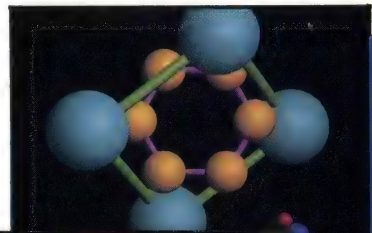
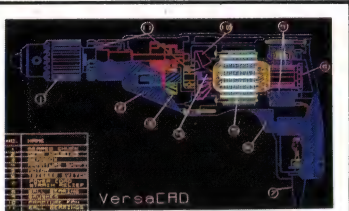
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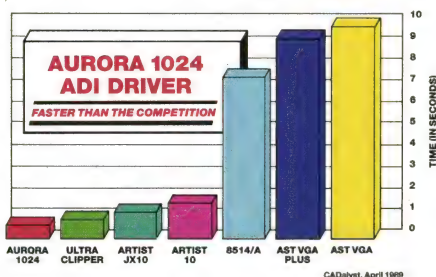
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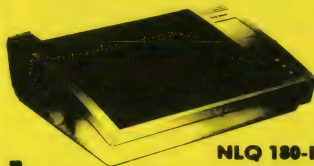
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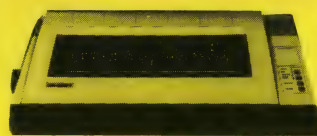
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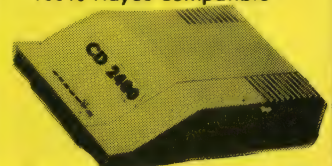
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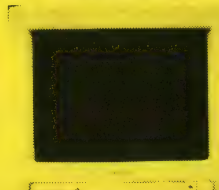
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INVENTING THE PC'S FUTURE

Architectural limitations could have the DOS world up against the wall without compatibility, technology, and design breakthroughs

Gordon A. Campbell

Several issues have to be resolved before personal computers will be able to perform better, faster, or more powerfully. One major concern is that certain barriers may have been reached and that going beyond them may require more than just a leap of faith. Jumping up to the next level of personal computer performance may not happen as quickly or as smoothly as the orders of magnitude of previous improvement took place.

During the past 25 years, chip technology has kept up with developments in associated device hardware and software. But after pushing the limits of personal computers to levels unthought of even a few years ago, the industry may have painted itself into a technological corner. It must now take the time to unravel some tangles that it has created in the areas of compatibility, silicon technology, and design expertise.

In part because of advances made in chip technology, the industry has been able to build higher and higher performance into microcomputers. This process of continual architectural innovation driven by silicon methodology—as

opposed to merely cranking up CPU speeds—will dominate the development of the industry-standard personal computer in the 1990s.

Anything You Can Do . . .

The computer industry evolved through three distinct phases. The first, really started by IBM, was the mainframe computer of the 1960s. The second phase

was the minicomputer of the 1970s, launched by companies such as Digital Equipment, Wang Laboratories, and Data General. Today the industry is firmly entrenched in phase three, the era of the personal computer.

Each phase of this evolution was based on a parallel development in semiconductor chip technology. This process is especially true in the IBM PC world, which is by far the fastest-evolving branch of the computer industry.

Throughout the 1980s, the PC-compatible world, including semiconductor suppliers, PC manufacturers, and PC users, has gone through some interesting technology transitions. In most cases, the transitions were driven primarily by the rate of productivity and the innovations present in silicon technology.

The first PC, as defined by IBM, processed approximately 100,000 instructions per second—about one-tenth of a MIPS (1 million instructions per second). In those days (the early 1980s) it cost about \$50,000 to put a theoretical 1 MIPS of processing power on your desktop. During the last five years or so, the suppliers of microprocessors, systems

continued



logic, and other PC system semiconductor components have driven the transformation from one-tenth-of-a-MIPS machines to 2- to 4-MIPS machines.

In the course of this transition, the cost of that theoretical 1 MIPS of processing power was driven below \$1000. In fact, some 80286-based machines now shipping already approach the \$500-per-MIPS point. By 1990, PC-compatible

machines may come with a standard 10 MIPS of processing power.

Sometime between 1990 and 1995, 100-MIPS PCs should arrive. This improvement in collective processing power will bring the cost per MIPS down below \$50. The dramatic drop from \$50,000 to \$50 per MIPS illustrates the orders-of-magnitude increase in productivity the industry has achieved (see figure 1). This economy of scale is one reason PCs have reached such a staggering level of sales.

The nose-diving cost of raw computing power is the result of two factors: progress in microprocessor technology and the growing numbers of manufacturers of integrated system logic, graphics, I/O, and communications chip sets.

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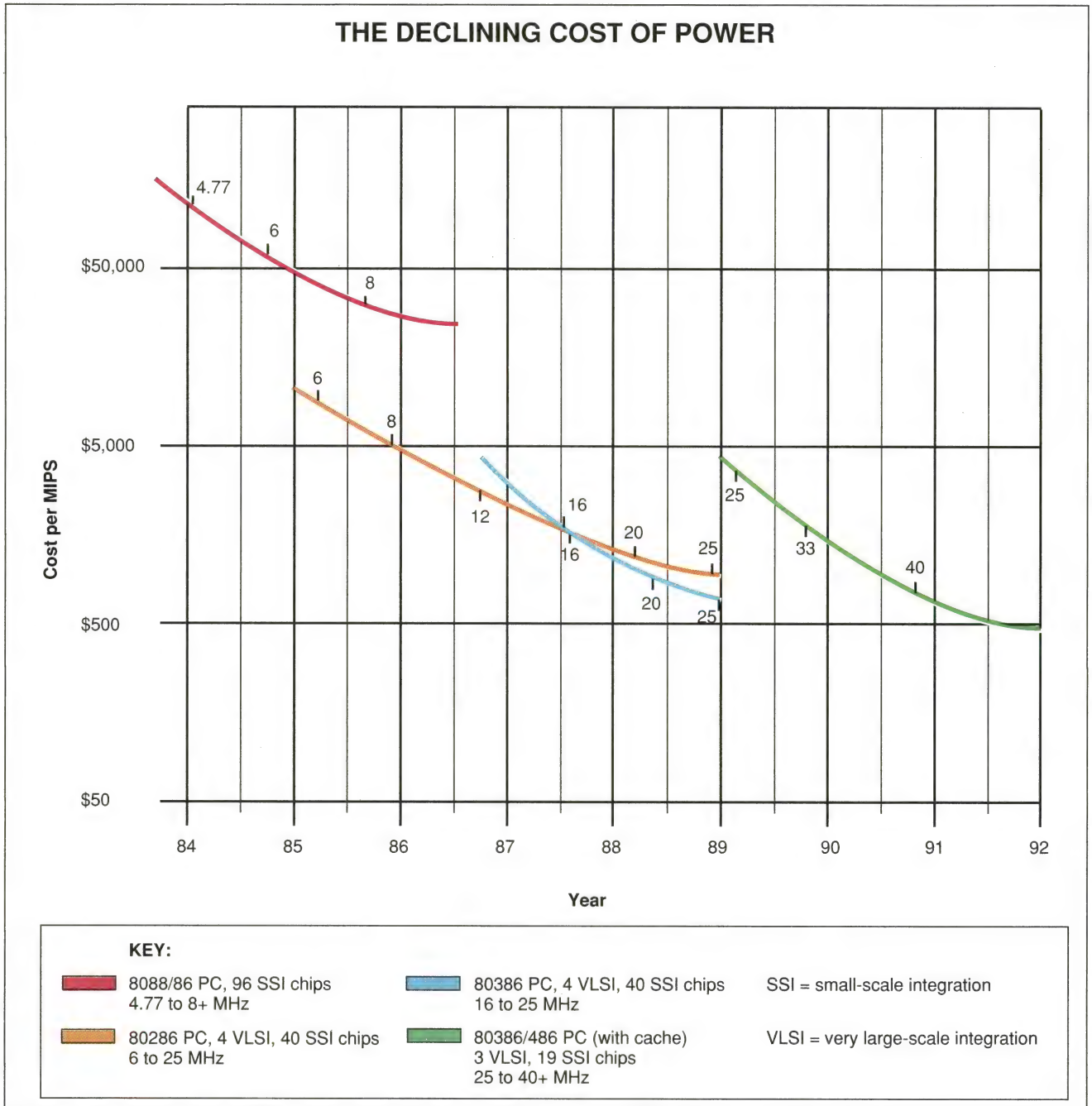


Figure 1: These curves represent processing power (in MHz and chip technology) and a PC time line. Succeeding generations of faster and more-complex microprocessors have married with ever-higher levels of integration to produce lower computing costs per MIPS.

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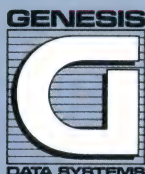
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Closely related to the importance of the microprocessor is the concept of the chip set. With this innovation, manufacturers were able to shoehorn the same logic functions onto five or fewer very-large-scale-integration (VLSI) chips, compared to the 100-plus small-scale-integration and medium-scale-integration chips that IBM had used to design the original PC.

The coming of the chip set not only

The
PC industry is now fully entrenched in the world of CMOS.

lowered raw silicon costs but also provided a way for manufacturers to easily and quickly bring new generations of PCs to market. The same concept was applied to graphics and is now being applied to I/O, mass storage control, and other PC subsystems.

Alphabet Stew

So far, the history of the PC, as expressed in the cost-per-MIPS model outlined earlier, has followed a predictable course: Through sheer manufacturing volume and by offering architectural innovations captured in silicon, silicon suppliers brought down the cost of building a PC.

What technologies are driving the silicon suppliers? The integration power of VLSI techniques rests on process technology. In the early 1980s, the semiconductor industry was really just starting to feel comfortable with its ability to integrate significant blocks of logic in a technology called negative-well metal-oxide semiconductor. NMOS was the first of the so-called MOS technologies, which have radically changed the semiconductor industry. MOS technologies differ radically from the previous power-hungry so-called bipolar techniques.

NMOS made it theoretically possible to manufacture thousands of transistors on a single piece of silicon without excessive thermal and power constraints.

When this technology was first put into place, NMOS was the highest-performance, cheapest way to manufacture transistors in an integrated block. However, a related technology called CMOS provided the technology to reach VLSI levels of hundreds of thousands of transistors on a chip and even ultra-large-scale-integration levels of over 1 million transistors on a chip.

During the same time frame in which the industry was moving into NMOS and CMOS process technologies, line-width technologies, which govern the actual physical dimensions of transistors, have moved line widths from around 2 to 4 mils down to 4 to 5 microns and, today, something like 1.5 microns and rapidly going to 1 micron. Beyond CMOS, a newer process technology known as Bi-CMOS (a hybrid of bipolar and CMOS technologies) promises to deliver both speed and the ability to integrate large numbers of transistors.

The 1-micron CMOS process barrier is a milestone in the semiconductor and PC industries. As they make the transition to 1-micron technologies, the possibility of producing the oft-talked-about single-chip PC becomes a practical reality. The 1-micron barrier is a true watershed for putting PCs into silicon technology. The technology is solid and is likely to have a dramatic impact.

The PC industry is now firmly entrenched in the world of CMOS. VLSI circuits are driving integration levels to the ultimate Holy Grail of single-chip systems. PCs with single-chip AT-compatible logic are due to begin shipping any day now.

The PC-compatible world is also just entering the ULSI world, which is usually defined as the ability to manufacture 1-million-plus transistors on a chip. One of the first examples is Intel's 80486 microprocessor with approximately 1.2 million transistors.

From the standpoint of PC-compatible users, one way to view all this rapid technology change is that when manufacturers were saddled with NMOS and line-width technologies of 2 to 5 microns, they could produce only one-tenth-MIPS machines, and the cost of 1 MIPS was very high. Today, as manufacturers are about to cross the 1-micron technology barrier, users have in their sights 10-MIPS processing power below the \$500-per-MIPS cost threshold. When less-than-1-micron process technologies are reached, manufacturers will see even more productivity gains, and the 100-MIPS PC will become a reality.

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What About Memory?

So far I have been discussing the logic side of the equation: microprocessors, systems logic, graphics, and so forth. The memory side of the equation is equally important, especially today with the advent of enormous, memory-hungry application programs and operating systems.

The early PCs were shipped with 4K-byte and then 16K-byte DRAM. Today, after the transition through the 64K-byte

DRAM generation, which was probably the briefest memory-density phase, the 256K-byte DRAM is the workhorse of the industry. And, although artificially high prices slowed down its acceptance somewhat, the 1-megabit DRAM is rapidly phasing in.

It did not take long for the 640K-byte memory barrier inherent in MS-DOS to become a headache; with PCs now routinely shipping with 8 megabytes or more of memory, the problem is compounded.

This has prompted many companies to develop both hardware and software solutions to enable users to transcend the 640K-byte barrier and be able to address, even with the lower end of the processor spectrum, large memory sizes in PCs. Future machines will be designed to accept many megabytes of memory largely because today's application programs are starting to demand more memory space for data and for the programs themselves.

One result of faster processors coupled with larger addressable memory space is that users can handle larger computing problems in more reasonable time frames. This leads to a need to improve the I/O to try to keep pace with processing power and available memory.

The I/O under the original definition of the PC being about one-tenth that of a 1-MIPS machine was fairly adequate. Then the AT came out, and it was about a 1-MIPS machine and, again, I/O wasn't really an issue.

But now that manufacturers have taken the original 6-MHz AT and boosted it to the 80286-powered machines that today run at up to 25 MHz, they have boosted theoretical throughput by an order of magnitude. The implication of this is that when you get that much additional processing power, more memory support and better I/O are required. Today, many of the old AT bus and XT bus structures effectively hobble the processing power.

With respect to I/O-bound performance, the most significant change is the transition at IBM from the old industry-standard architectures of the XT and the AT to the new Micro Channel definition. With Micro Channel, IBM provided much better I/O capabilities and a bus definition that had the flexibility to do things that the old bus structure could not, such as bus mastering.

The adoption of the Micro Channel was not only an attempt to address I/O problems, but also a major transition on IBM's part. In essence, the introduction of the Micro Channel represents IBM's recognition that the adoption of mainframe computer architectures was required to keep up in the PC performance race. Today throughout the industry, sophisticated mainframe techniques are migrating down to PCs. Mainframe techniques, such as cache memory subsystems, have now become a common item on PCs. Other mainframe techniques will also be applied to the PC, especially in the area of I/O processing.

The challenge for all the PC silicon

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suppliers is to adopt mainframe techniques and recast them into fast and inexpensive silicon. For example, cache controllers must be integrated into the other elements of the PC system logic. At Chips & Technologies, we have integrated both the cache controller and the DRAM controller onto the same chip as the CPU controller. Other companies (e.g., Intel) have taken different approaches.

Cache architectures are clear indicators of the migration of the mainframe to the desktop. The significance of the cache is that, as we push PC architectures up into the 16-, 20-, and 25-MHz performance ranges, there is a need for more efficient memory management.

The key to this process is to deliver the benefits of advanced computer architecture and still drive down costs. In contemplating the role of silicon in the mainframe approach to PC design, it is important to realize that, unlike the mainframe, power and size constraints will require even greater emphasis on sophisticated CMOS process technologies.

Most mainframes today derive much of their speed and throughput from the widespread use of emitter-coupled-logic circuits. ECL is blazingly fast but imposes a heavy penalty in terms of power requirements and thermal dissipation.

The PC's success is due to the fact that manufacturers have managed to push performance levels while also incorporating direct cost improvements. Most cost contributions have come from the ability to do higher levels of integration and performance in fewer CMOS chips.

Semiconductor technologies offer a wide and almost unlimited range of performance. But in the PC world, it is a requirement to adopt the technology that will continue to drive the relative dollars-per-MIPS curve downward.

Process technology and semiconductor chip design are the basis of the PC industry. And there is a fair degree of commonality across product lines ranging from powerful server-type machines to emerging notebook computers.

For example, the rush in the laptop arena is to produce thinner and thinner machines. To support that, you will see laptops go in a couple of different directions. One will be an improvement in terms of thinness and weight; another will be support of VGA-quality graphics and 16 shades of gray and black-and-white and, ultimately, support of 16-color LCD with VGA resolution.

This class of machine requires extremely high levels of integration: single-chip logic systems, single-chip graphics controllers, single-chip power supply

controllers, and so on. Laptop manufacturers are relentless in their pursuit of integration, and the semiconductor industry is responding in kind.

Then there will appear, on the very low end, techniques such as those combining several ICs in one package. This advanced packaging technology is now in demand to support what is being called the "pocket computer." In this case, single-chip integration is insufficient; advanced packaging techniques are required.

Probably the two most significant trends in the PC world are the drive for higher levels of integration and the sudden rise of alternative microprocessors. The 8086 architecture has matured through the 80286, the 80386, the 80386SX, and now the 80486. Today the 80286 continues to be the workhorse of the single-task, single-user market and will most likely be so for the foreseeable future. The 80286 market will probably not grow a lot but will continue to be a high-volume segment of the overall market. At the slightly higher end, and particularly in machines where people want better communications capabilities, networking, and coupling capabilities, I expect to see the 80386SX as the highest-volume microprocessor, followed closely by the 80386, and that followed closely by the 80486.

Currently, several RISC-based machines are making a play to become a factor in the PC world. Basically, these microprocessor architectures are coming out of the workstation world with the ability either to do software emulation of MS-DOS packages or to actually include an Intel-architecture microprocessor in the computer.

Although interesting, I don't think that these software-emulation capabilities will ever be successful as a commodity product. There are too many compatibility problems in that approach, and speed will remain an issue.

However, I do believe that some hybrid machines will appear that can support both Unix and DOS. It is likely this approach will have some common hardware, but largely separate processors.

In the near to medium future, I think that a number of different developments will ultimately lead to a dramatic change in PC architectures. One clear trend is that just by pushing the clock speed in some current microprocessors, 8-MIPS machines based on 33-MHz 80386 microprocessors and 10-MIPS machines based on 40-MHz 80386s become feasible. Now that the 80486 has introduced a

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different microprocessor architecture that allows almost a doubling of performance, I expect to see 80486 machines that will support between 15 and 20 MIPS in the main processor.

However, one thing that will happen is that the use of accelerators, floating-point processors, graphics processors, and communications processors will increase. It should come as no surprise that the coupling of all that silicon will result in a machine that has 50 to 100 MIPS of

fully compatible processing power.

That is what I would expect to see happen on the PC side. On the workstation side, I think we're going to see RISC architectures that are inherently very fast, powerful processors pushing up easily into the 100-MIPS range. The interesting question to ask is, when will we hit the wall in terms of pushing clock speeds? In the case of the PC, somewhere in the 40-MHz range is probably getting close to the top end of the spectrum.

This scenario is likely to develop for two reasons. The first problem concerns the silicon technology and the sheer complexity of designing and manufacturing the part. Submicron process technologies are not trivial undertakings, and the design methodology of advanced semiconductor devices is becoming more complex.

The second problem is that the industry is trying to build these super-PCs on plain old cheap PC boards using as few layers as possible. In the case of a main-frame product that runs at 60 or 70 MIPS, much of the design expertise is devoted to issues such as special kinds of terminations and special techniques used to reduce ringing, radio frequency generation, and other technical problems that are related to extremely high-frequency electronics.

The upshot of this approach is that PC board technology and current silicon technology may limit the speed of PCs to less than 50 MHz. A different architecture is needed to further increase the productivity of the PC. A possible solution is the approach being taken by some current manufacturers of workstation architectures. These RISC-based machines offer more MIPS than the Intel architecture can provide.

PCs with multiple processors could appear as early as 1990. A true multi-processor architecture will dictate some dramatic changes, especially in operating systems. In the area of graphics, for instance, there will be development and integration into the PC of not just graphics processors, but accelerators and graphics management chips as well. These chips will be dedicated to supporting performance and productivity in those specific areas.

A major caveat in this scenario is compatibility, which is pretty much taken for granted today. The likely evolution of graphics accelerators and other hardware accelerators will once more raise compatibility as an issue.

Compatibility was, and continues to be, the foremost issue in the PC business; users can't reap the benefits of higher performance or lower cost if they don't have compatibility. As performance is enhanced, compatibility becomes an architectural issue. So far, the industry has successfully adapted the architecture to accommodate higher performance. ■

Gordon A. Campbell is president and CEO of Chips & Technologies in San Jose, California, a company he founded in 1984. He can be contacted on BIX c/o "editors."

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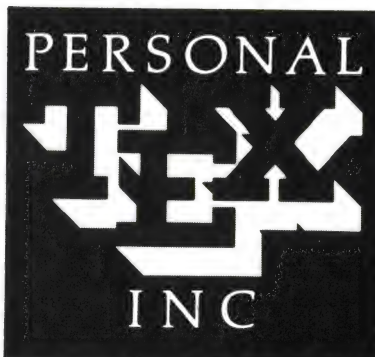
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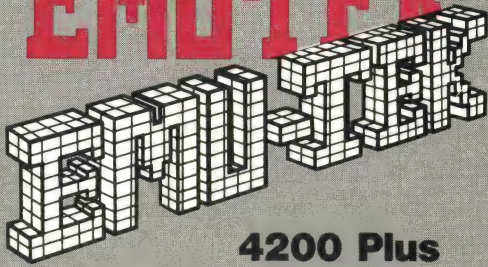
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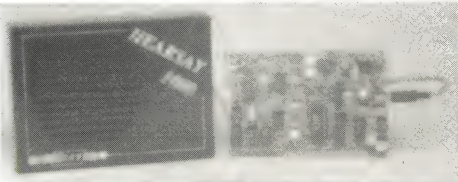
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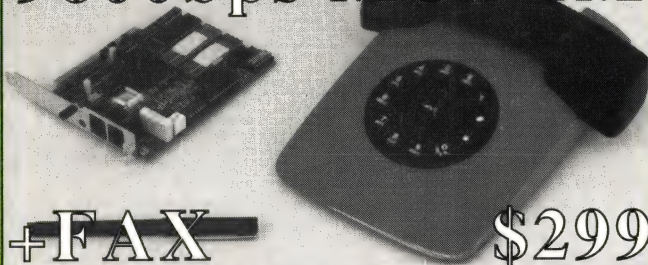
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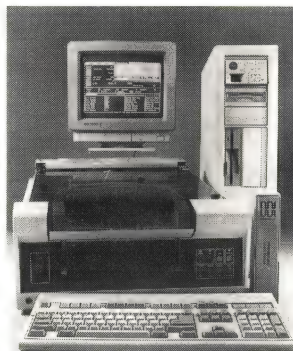
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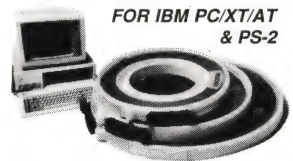
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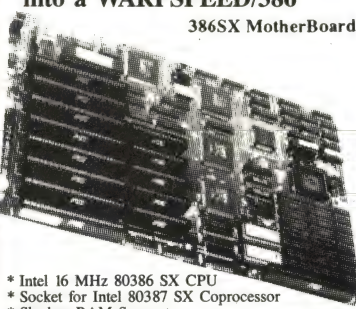


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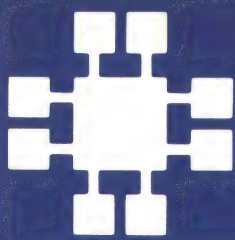
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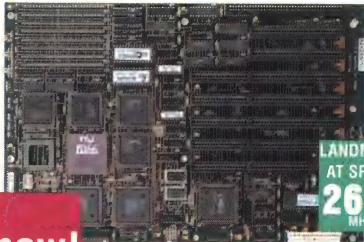


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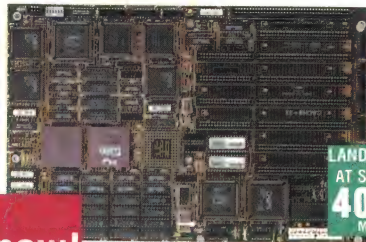
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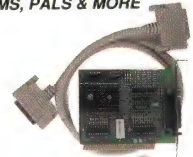
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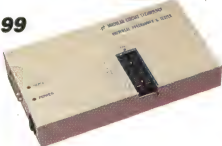
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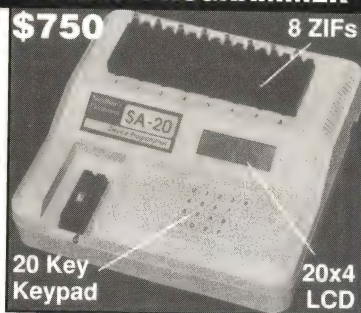
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THE STATUS OF APPLICATIONS SOFTWARE: LATE

BYTE's software reviews editor offers his views on the widening gap between hardware and software

Dennis Allen

If you've ever set out to accomplish a particular task on your PC only to find there was no software that could do it, you've experienced *software lag*. It's a frustrating feeling—knowing that your computer is capable of doing what you need but is prevented from doing so by the lack of the right software. You've been cheated. The computer that once promised so much now has so little to offer.

The root of the problem is forked. Neither IBM nor Microsoft has provided a 32-bit DOS-compatible operating system, and developers are still learning how to cope with many megabytes of data. As a result, the current crop of applications software often relies on brute force to get things done.

Not everything, however, is bad in the software world. In fact, there is evidence that applications software is headed for a common user interface, and that WYSIWYG may become a way of life. And programs may even be getting smarter.

Although you don't need a crystal ball to predict that new changes in software are coming, exactly what the changes

will be is less clear. But you can identify some of the forces driving the changes. The one thing that is certain is that users know what they want.

The Operating-System Bottleneck

Of course, not all the fault for the software lag belongs to applications developers. They're missing an operating system designed specifically for 80386-based

hardware. Although OS/2 happens to work on 80386 systems, it was not designed for them. It's a 16-bit operating system for 80286 machines.

On the other hand, developers have yet to conquer OS/2. Even the grandest application of them all—Lotus 1-2-3 release 3.0, which took years to produce—was designed for DOS 3.x. You'd be hard-pressed to walk into any computer store and find five OS/2 applications sitting on the shelf. A lot of software companies talk about OS/2 applications, but few have actually produced any.

The reasons offered are many, but it all boils down to a matter of investment. While OS/2's complexities, such as multitasking and data sharing, ultimately offer more headroom for sophisticated programs, its learning curve for developers is more like a brick wall.

Even the software giants such as Lotus, Ashton-Tate, and Microsoft, with their abundant resources, have experienced setbacks. Just consider the long waits for 1-2-3 release 3.0, dBASE IV, and a full-featured Windows word processor. And those are just DOS-based applications. The

continued



point is that, even for these companies with their millions of R&D dollars, the number of labor hours needed to develop sophisticated applications is gargantuan.

Managing Megabytes

To complicate matters further, increased storage capacities have offered new opportunities and challenges for applications developers. While more storage would seem obviously better, not everyone is certain how best to use the hundreds of megabytes that optical drives provide.

For now, publishers are using CD-ROMs to provide static reference materials. Notable examples are Grolier's Electronic Encyclopedia and Microsoft's Programmer's Library. But what most users really need is for their applications to manage dynamic archiving.

Currently, when your hard disk becomes nearly full, you have to remove your older files. Maybe you archive them on floppy disks. If you do, chances are that you don't bother referring to those files again because it's too much trouble: You would have to fumble through all your archive disks, trying one and then another, to find a certain bit of information. You might even find it easier and faster to search through printed reports in a file cabinet.

That's one of the ironies of today's applications software. Although most of the modern world is convinced that you can do record keeping and manage things better on personal computers, you still have to resort to a file cabinet and Penda-flex folders to see your old records.

A better arrangement would be applications software that really takes advantage of read/write or WORM (write once, read many times) optical disks. Such software would, on a regular basis, archive your old records and files on optical disks. More important, the application program would manage those archives. It would continually update its indexes so that, say, five years from now, on a moment's notice, you could call up the spreadsheet for October 1989's production costs. If you needed to change optical disks, the program would tell you which one to insert.

Also, your application should be able to use that archived information. It should be able to correlate it with more recent information to generate comparative reports and to project the next year's performance.

Unfortunately, that kind of software does not exist today, even though the hardware to handle such tasks exists. The fact is, software for dealing with large amounts of on-line data is just emerging. Consider Lotus Magellan and Traveling Software's ViewLink, for example. They are the first major attempts to help you actively manage several megabytes of disparate information. Either will let you peer into data files on your hard disk and view the data in its native format. Both will also search your hard disk for the file or files containing specific information.

But while Magellan and ViewLink work fine as utilities for managing what's currently on your hard disk, they're really no help at managing ar-

chives on floppy disks. Both would also fall short in handling a gigabyte or more of data on optical disks. Even worse, both of these programs create a whole new set of problems. Magellan takes up valuable hard disk space with its index, and it needs to update the index frequently, sometimes taking several minutes to do that. And because ViewLink doesn't use an index, its searches can take a long time if you're working with a large disk with lots of data. Equally as bad, there are no Magellan or ViewLink equivalents for Windows or Presentation Manager (PM).

Calling on Brute Force

Also considerable is the muscle needed to run the current crop of software. Most of us have traded in our 8088-based systems for 80286s, and many have already traded their 80286 systems for 80386s. We do this to get merely adequate performance, while none of the software really takes advantage of the 80286 or 80386 architectures. Even worse, as we move up to systems that are more powerful than were thought possible just a few years ago, we still find ourselves waiting: waiting for AutoCAD to regenerate a complex drawing; waiting for 1-2-3 to recalculate a large spreadsheet; and waiting for Lotus Agenda to stop fiddling with the heads on the hard disk drive.

Agenda is a good example of the problem. Like other high-powered applications, Agenda is sophisticated and complex, and it demands an extraordinary amount of computing muscle. Yet aside from the brute force that it commands, it

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THE STATUS OF APPLICATIONS SOFTWARE: LATE

doesn't really take advantage of the features that 32-bit hardware offers.

Just to use Agenda, you have to devote a lot of time to learning it. In return, it organizes information like no other software—making lists and doing mundane chores for you automatically. It does so much that, in its relentless scans of your data looking for something it should do, you're left with a computer that responds with all the speed of a snail.

So here we are, using high-powered 80386-based systems (and probably 80486 systems, soon) to run applications that were designed years ago and written for 8088-based systems. Software developers for the PC have been somewhat ambivalent toward OS/2 (and toward Unix, for that matter), and they've been less than eager to commit to using the Micro Channel architecture. Rather than write applications software directly for these high-powered systems, developers have instead sought to extend DOS, "enhance" memory, and employ various other tricks.

But users expect more, and, in fact, they need more. They need programs that can manage several tasks at once so that they don't have to. They need programs that can work without conflict in a heterogeneous environment of applications. And they need software that can work with other software, sharing information and files.

The Common Interface

Applications are making progress in the area of user interfaces, however. Call it Mac envy, if you like—PC users liked what they saw on Apple's Macintosh. The Macintosh's graphical interface with pull-down menus was exactly what the corporate world had been looking for: an easy-to-learn system. For businesses, the time and expense for training people to use PCs has soared with no ceiling in sight.

None of this is news, really. It's just that the Mac proved long ago that personal computers could be made easier to learn and use. But in those early days of the Mac, there was no such interface for the IBM PC. Turning to the next best thing, the corporate world embraced simple menuing software that simply worked as a DOS shell to launch other applications. Programs such as Magee Enterprises' AutoMenu filled a void left by the software giants.

Meanwhile, virtually every application began to take on parts of the Mac interface. In many cases, developers simply added menus. Unlike the Mac, however, the PC had no standards for

menu styles. So some programs imitated 1-2-3's menu format, calling it a de facto standard. Others went further and provided pull-down or pop-up menus. Applications became easier to use, but for the most part, they were all different.

Then came Digital Research's GEM and Microsoft's Windows. After several years, it appears Windows has gained a toehold in the PC market. Corporate buyers wanted PM for OS/2, but until it became available they saw Windows as a logical stepping-stone. The attraction was that businesses could develop their in-house applications on Windows today and later adapt them to PM for OS/2.

Now, that corporate strategy is beginning to pay dividends to individual users. Because of the significant number of systems running Windows in the corporate environment, developing applications for Windows is more attractive to developers. Granted, the number of Windows programs so far is small, but the group includes some really heavy hitters, such as Aldus PageMaker, Micrografx Designer, Samna Amí Professional, and Microsoft Excel.

While the number of Windows programs is growing, it's not by leaps and bounds. Although the user interface issue has been all but resolved, applications developers, worried about the fluidity of the software market, have been riding the fence between developing for Windows and developing for OS/2. From their point of view, developing for both simultaneously isn't practical. They need to get their software products to market as quickly as possible to compete, and they need to concentrate their efforts; they can't afford to have half a development team working in OS/2 and the other half in Windows.

You might say that developers have learned a lot from Lotus's experiences in trying to develop its 1-2-3 for a multitude of platforms. The resulting delays have cost that company more than just a little overtime: Lotus also suffered a loss of credibility, which was reflected in the stock market.

It all comes down to this: Today's applications software for the PC is only inches away from a common user interface. Although it seems inevitable that in time that goal will be reached, it may not happen as quickly as users would like.

Going in the Right Direction

In other areas, applications developers have made more headway. Consider the WYSIWYG phenomenon. Page-layout systems such as Aldus PageMaker and

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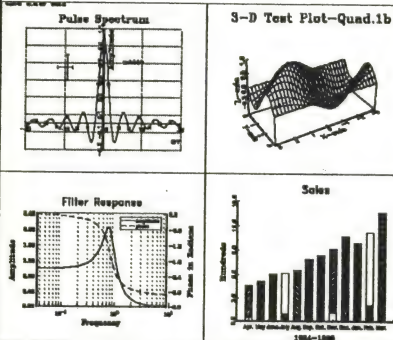
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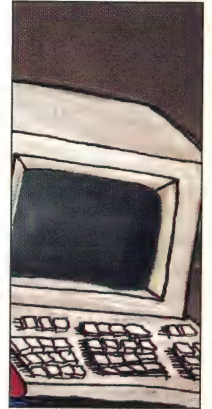
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Because of the significant number of systems running Windows in the corporate environment, developing applications for Windows is more attractive to developers.



Xerox's Ventura Publisher have been the catalysts. Although WYSIWYG on a PC had been possible before, for many people those were the pioneering programs. As page-layout programs, PageMaker's and Ventura Publisher's existence depended on WYSIWYG.

Other applications have followed suit. In fact, a whole subgenre of software—presentation graphics—faces near extinction merely because word processors, spreadsheets, and other applications have incorporated WYSIWYG presentation features.

It's really no wonder. After all, presentation counts for a lot in today's society. People give presentations to sell both goods and ideas. Strangely, though, many word processor developers try to skirt around the WYSIWYG issue, saying that users don't actually need WYSIWYG during the writing process and that users only need to see monospaced characters as they create text. Their argument is that you can go back later and make the whole thing look the way you want it to.

In truth, that argument is just smoke to hide the fact that most word processing software is simply too slow to work in WYSIWYG mode as you type. That's partly the fault of developers overburdening their products with a list of features so long that no one can remember or use them all. Each of those features steals precious memory and execution speed from the application. So, you end up with a word processor that can do many things you'll likely never ask it to do but cannot show you how your printed page will look—that is, of course, unless you exit the edit mode and enter the graphics mode to view your work, and then exit the graphics mode and enter the edit mode to continue writing. How silly the whole process is—to treat one computer as if it were two machines, one for writing and the other for layout.

There is, however, at least one notable

exception. Samna's Amí lets you write and edit in WYSIWYG mode. It's also the first real word processor for Microsoft Windows. Others will certainly follow, and among them will be an offering from Microsoft itself as well as an enhanced version of Amí (Amí Professional). Another similar program, Lennane's DeScribe Word Publisher, is under development for OS/2 PM.

Advancements in Number Crunching

Another area of software that's been moving forward is number crunching. Spreadsheet applications have matured somewhat, and users have recently witnessed the emergence of a whole new generation of spreadsheet software. Generally, the most significant improvement is the three-dimensional worksheet, which lets you work on several worksheet pages at once. More and more of the major spreadsheet programs are offering that feature.

However, only one relatively new spreadsheet, FormalSoft's ProQube, provides true 3-D manipulation. Instead of simply letting you calculate separate pages, ProQube also lets you view your spreadsheet data from any aspect—front-to-back, side-to-side, or top-to-bottom. Imagine, for example, that you have a worksheet page for each month of the year, and that it calculates your profit or loss. Each of those pages would use the same template, and if you stacked one on top of another, you would have a "cube" (actually a block) of spreadsheet cells. Viewed from the front of this imaginary cube, each layer of cells would represent a particular month.

Any so-called 3-D spreadsheet can handle that task. But with ProQube, you can rotate the imaginary cube of data to view, say, the net profit from each month of the year. Or, from another angle, you might view the net profit for the month of May for each of the last five years.

THE STATUS OF APPLICATIONS SOFTWARE: LATE

Admittedly, with a little time, you could program formulas in any other spreadsheet to accomplish the same tasks. But the conceptual difference is quantum. ProQube lets you play "what-if" in a new way—one that requires less work on the part of the user. ProQube is a real attempt at handling human perspectives of spreadsheet data.

But spreadsheets are not the only application area where number crunching is being pushed. Another, perhaps less obvious, application is CAD. A sophisticated CAD package typically places more demands on a computer's mathematical abilities than any statistical analysis or equation solver package.

While 2-D drafting products, notably AutoCAD and others like it, have been around for some time, only recently have solid modeling packages become available. The difference is that the latter lets you construct objects with blocks, cones, spheres, and cylinders.

Let's say, for example, that you need to draw a hole for a vertical vent pipe that goes through the roof of a house. That's not as simple as it might sound. Because the roof is slanted and, therefore, the pipe is not perpendicular to the roof's plane, the hole is not a perfect circle. And trying to calculate the precise shape and size of the elliptical hole is not trivial. That's where solid modeling comes in. Instead of drawing a hole, you create a cylinder the size of the vent pipe and then simply place it through the slanted roof. Then, through what's called geometric subtraction, the solid modeling program can erase the cylinder (and everything that was in its way), leaving a perfectly shaped ellipse.

From the user's view, it's all quite simple, and it simply makes sense. Underneath it all, however, an awful lot of computations are made. For now, you can only find solid modeling systems at the high end of the CAD spectrum. But in time the technology will likely sift down to applications such as graphics design packages.

Future Applications

Understanding where we are in applications software is, of course, only a prelude to knowing where we're going. In time, developers will overcome the obstacles of the hardware-software gap and the operating-systems bottleneck and will adhere uniformly to a graphical user interface. The resulting applications software will no doubt reflect the tradeoffs and compromises that are made to achieve those goals.

In addition, market-based external in-

fluences will affect applications software, but they may not be what you think. What will greatly affect U.S. applications software development is the foreign market—in particular, the long-awaited European community market.

The European market after 1992 will cause two major changes. The first that users will probably see will be created by the vast new opportunities for U.S. software firms to sell their products in Europe. Although software developers will face the problem of writing programs for many languages (in fact, many already do), they will also begin to produce applications that have more "global" characteristics.

Until now, most software written in the U.S. has been specifically tailored for U.S. tastes. It directly reflected feedback from U.S. users and their work habits and concepts. But as the European market becomes more important to U.S. software developers, it stands to reason that future applications software will reflect the needs of European users, too.

The change will probably be subtle. Since users may all be introduced to new and sometimes better ways of accomplishing their tasks, eventually much good will probably come of this gradual change. On the downside, there is a risk that developers will tend to overburden programs with even more features.

The second change caused by the new European market may come about more slowly, but it could be much more significant than the first. That change will be the emergence of large European-based software development houses. In fact, European-based companies will be the first to benefit from the new trade regulations there. Small but established software companies will suddenly have easier access to a much wider market—one that's based in their own backyard. That opportunity will inevitably lead to growth in European-based software companies, and that growth will thrust them into a strong position for entering and succeeding in the U.S. market. It could be that the next Lotus- or Microsoft-like software giant will be one that's based in Europe.

Then there is another external influence to consider: the USSR. So far, the only software to come from the USSR is a game, Tetris, but that may soon change; in fact, one U.S.-based company is already planning to introduce an expert system that was developed in the USSR. With trade restrictions lifted for exporting 80286-based computers to the Soviets, along with the Soviet desire to

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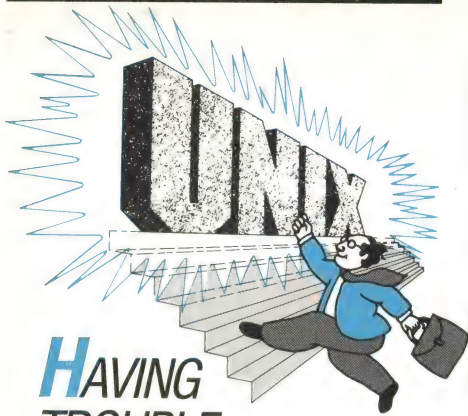
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become a leader in world trade, you can expect to see more Soviet-based applications in the future. The first Soviet software will probably be Americanized applications based on Soviet-developed software engines. Such is the case with the soon-to-be-released expert system. The U.S. company is taking a Soviet-developed expert-system engine and adding a practical application interface for financial modeling.

The real wild card, however, is Japan. So far, largely because of cultural differences, Japan has found the American software market impenetrable. It's not that Japan isn't trying, though. The Japanese microcomputer industry is working on a new universal operating system, called TRON, and a new system of distributing software electronically—via phone, radio, and even vending machines. If either effort materializes, Japanese software companies will find themselves in an enviable position that could allow them to dominate the applications market. Their plan is grandiose and perhaps unattainable. But given Japan's past successes in identifying, penetrating, and ultimately controlling world technology markets, the possibility of continued success is very strong.

What the World Needs Now

Aside from those external market forces, just where should applications software be headed? In a nutshell, applications need to be smarter and easier to use. You should not have change your way of thinking and conform to the way a particular application program does things. Tasks that are obvious should be done automatically. And the user interface should allow instinctive choices.

We need to see more programs like Lotus Agenda that are smart enough to do things automatically. Agenda is nearly miraculous in the way it can take free-form information and automatically categorize it; independently create project reports, to-do lists, and tickler files; and make associations between otherwise differing subjects. In those respects, Agenda comes the closest yet to imitating a top-notch personal secretary.

But for all its glory, Agenda is slow, and learning to use it is slower. In fact, one piece of Agenda folklore claims that White House Chief of Staff John Sununu, a personal computer enthusiast himself, considered Agenda for the Bush transition team. But the learning curve was so steep, and time for the transition team was so short, that Agenda was discarded in favor of another, simpler program.

We need more programs like Business

Forecast Systems' Forecast Pro, a statistical forecaster that brings sophisticated mathematical formulas within reach of nonstatisticians. Forecast Pro has its own expert system that analyzes your data and then applies an appropriate forecast model. Before Forecast Pro, it took a real expert—someone with a degree in statistics—to choose and run the correct mathematical model just to project a company's business income.

We need more programs like ProQube that let us view our numerical data in ways that make sense to us, not just to our computers. Likewise, we need CAD and graphics design software that take advantage of solid modeling. Moreover, we need solid modeling software that allows the objects we create to have real-world characteristics. That way, when we design something, we can test its strength and function in the real world without resorting to a separate analysis program.

We also need applications that integrate other applications. Forget the dream of all-in-one applications for word processing, database management, spreadsheets, and so forth. Those integrated packages are nothing more than modern-day jacks-of-all-trades in a world of specialization. It's just plain smarter to buy separate programs that precisely fit your needs. What we really need is a new breed of software that can oversee all those separate applications: a kind of intelligent shell that watches over your work, learning your routines.

Let's say that every month you extract the sales data from your inventory system and import that into your forecaster to project next month's sales; then you import those projections into a spreadsheet to do your financial planning; and then you generate a report with your word processor to reflect the outcome. An intelligent shell would recognize the pattern and do the tasks for you at precisely the same time every month. When such intelligent software finally exists, all you will have to do is remember to leave the computer turned on.

The sad thing is that the personal computers that we have today, particularly the 80386-generation systems, can handle the job. But our present-day applications software, spawned by the 8088-based generation, is generations behind, and newer and better hardware is on the way. The unfortunate truth is that we cannot escape the generation gap. ■

Dennis Allen is a senior technical editor for BYTE. He coordinates reviews of applications software. You can reach him on BIX as "dallen."

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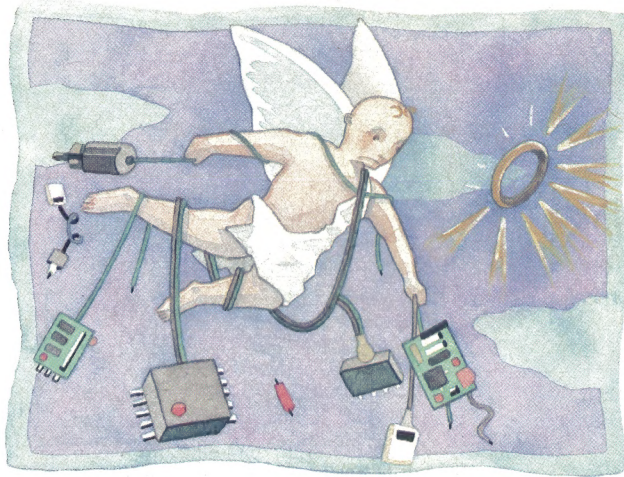
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THE WAGES OF SIN

What price has the IBM PC world paid for its compatibility?



Intel has released the 80486. A fine piece of work, it manages to put a complete 80386 system—80386 processor, 80387 FPU, cache, memory management unit, and so on—onto a single chip. And not only that, but to substantially improve the performance of the various bits, the 80486 takes fewer clock cycles than the 80386 to do the most frequent instructions. At constant clock rates, the 80486 is faster. The 80486 version of the 80387 is quicker than the real 80387, too. Not to mention that you get an 8K-byte cache (one-eighth the main memory of most early PCs) on-chip.

It is clear that the decision to make the 80486 an integrated 80386 system was not made by accident. It does nice things for users; it offers higher performance, a lower chip count, floating-point, lower power, and higher reliability. And all the 4.77-MHz 8088 software designed for 64K-byte machines will still work.

The 80486 does nice things for Intel, too—the company doesn't need to worry about losing a slice of business to 80387 copiers (the math chip is built in), other cache controller vendors (ditto), or 80486 cloners (since copying the whole CPU is a serious undertaking).

The 80486 is a goody to vendors of high-end machines, as well; all they need to do is take a well-designed 32-bit 80386 system, make a few (if any) changes to the design, and stick an 80486 into it. The result is a powerful new com-

puter with an established software base, and the whole thing costs no more (and perhaps less) to make than an 80386. Moreover, it can attract a much higher price by virtue of its 80486-ness and higher performance. Everybody wins, right?

Well, no, they don't. The big losers are the users who buy the machine—because they have always believed the story about maintaining their “investment” in software. They have always fought for (and bought) a new machine that runs their old floppy disks, unchanged. As a result, they have bought themselves the dead weight of decade-old technology. The 80486 involves a fair amount of circuitry; how much of it is there simply to make the beast 8088-compatible, we can only guess. But we do know that when other companies have made machines—or microprocessors—that didn't have to be 8088-compatible, they produced designs that used many fewer transistors to go much faster. INMOS's T400 family uses about as many transistors as an 8086 but keeps pace with an 80386. Sun's SPARC architecture (in its various guises) and MIPS's R2000/R3000 processors use more transistors than an 80386 for much higher performance. And now, the 80486 isn't even the fastest machine that Intel produces.

Indeed, the 80486 is the slowest of the three high-performance introductions this year. The most prominent of these was the 860, which, despite being gross-

ly overhyped by the rumor mill (and, possibly, by Intel's marketing) is easily twice as fast—and perhaps three times as fast—as the 80486. And the new member of the 960 family, which tries to execute three instructions per clock cycle under reasonable conditions, is much faster than the 80486.

Yes, IBM PC/MS-DOS fans, your addiction to the past has cost you a drop in performance of 50 percent or more. If you had been happy to eschew the past when better machines turned up, you wouldn't have encouraged the software vendors to live in the past. Then, perhaps, they would have decided that there was real money to be made in portable software. Manufacturers might have created operating systems that added new and useful facilities (such as graphics) but that were simple and clean enough not to be bound to just one proprietary piece of hardware. (Of course, too much silliness in the operating-system spec would have been ignored by the software vendors.) Then you could have bought this year's smart new machine with the assurance that your old software could be upgraded to the new machine for a nominal fee, and we'd all have much nicer, faster—and probably cheaper—computers than we do. ■

Pete Wilson is a senior engineer at Prisma, Inc. (Colorado Springs, CO). He previously worked on the design team for the INMOS transputer.

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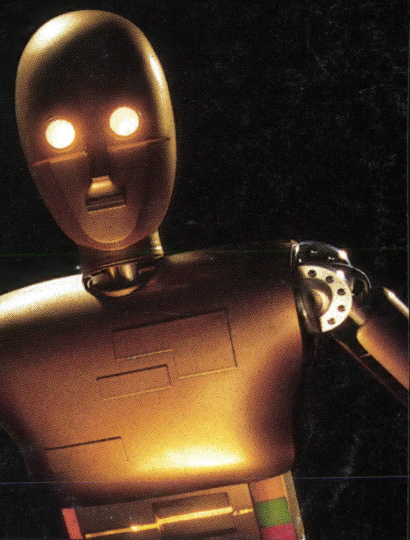
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